


PG141-D00

GA104 GB5-256 DESIGN, 8GB GDDR6X, 256b, X16
DP + DP + DP + HDMI/DP

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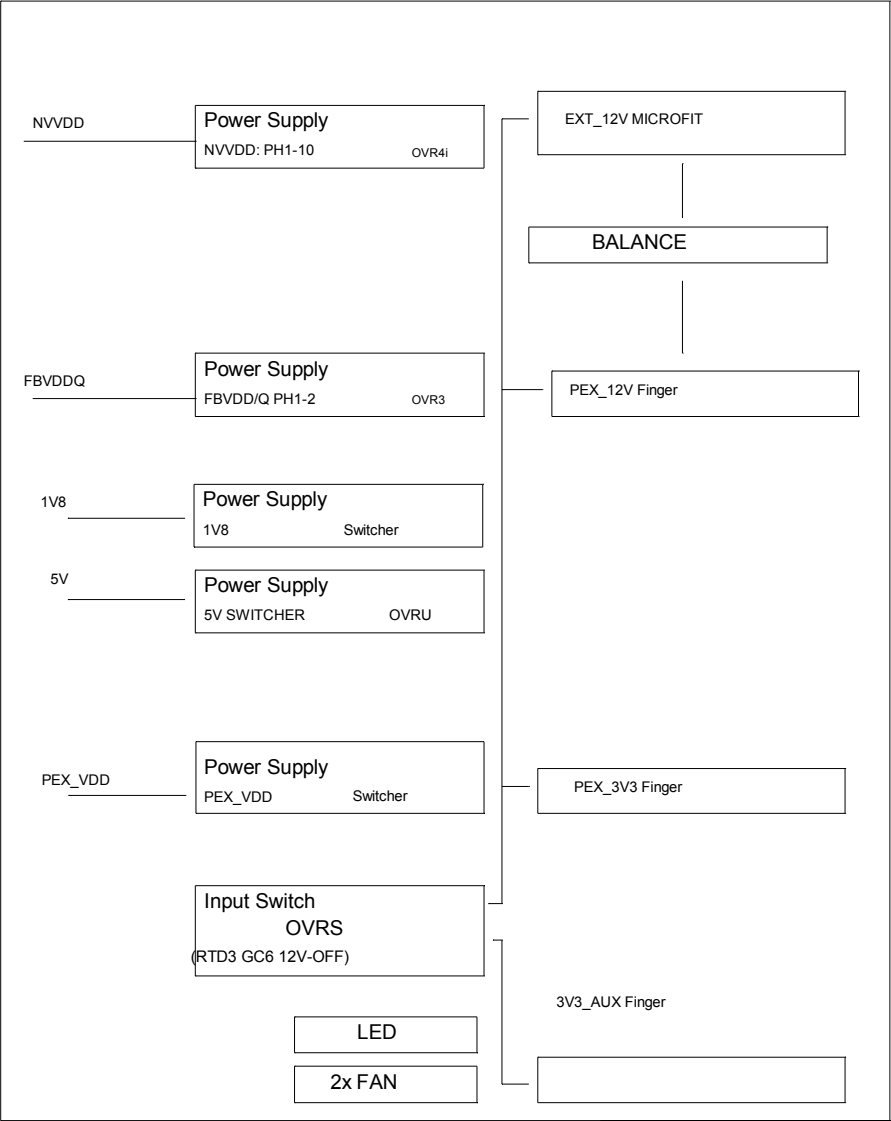
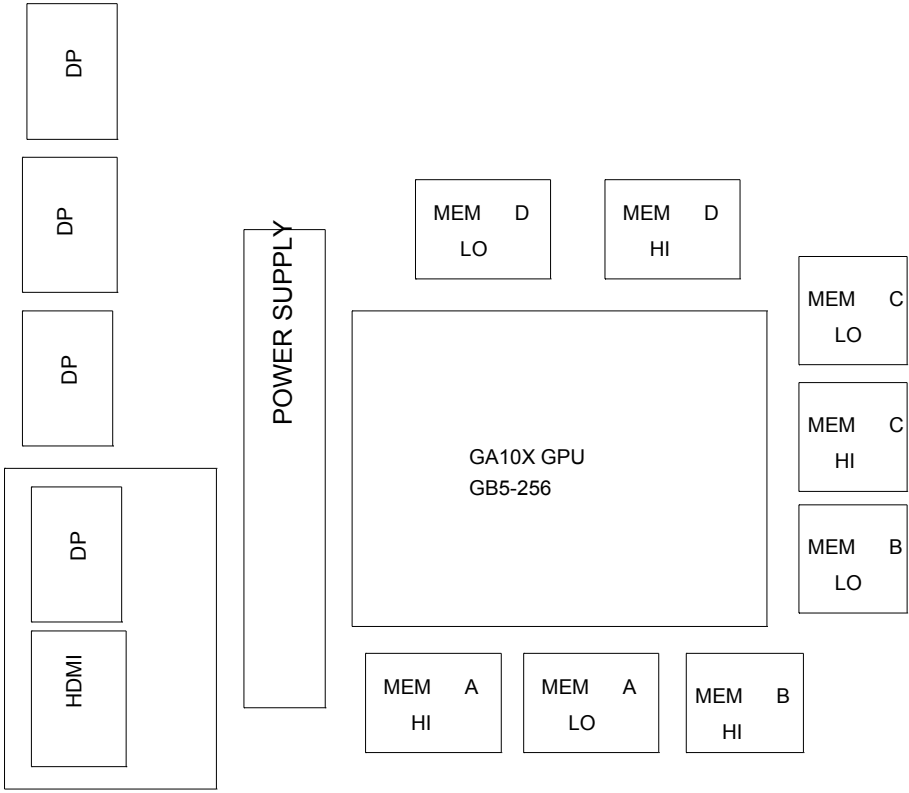
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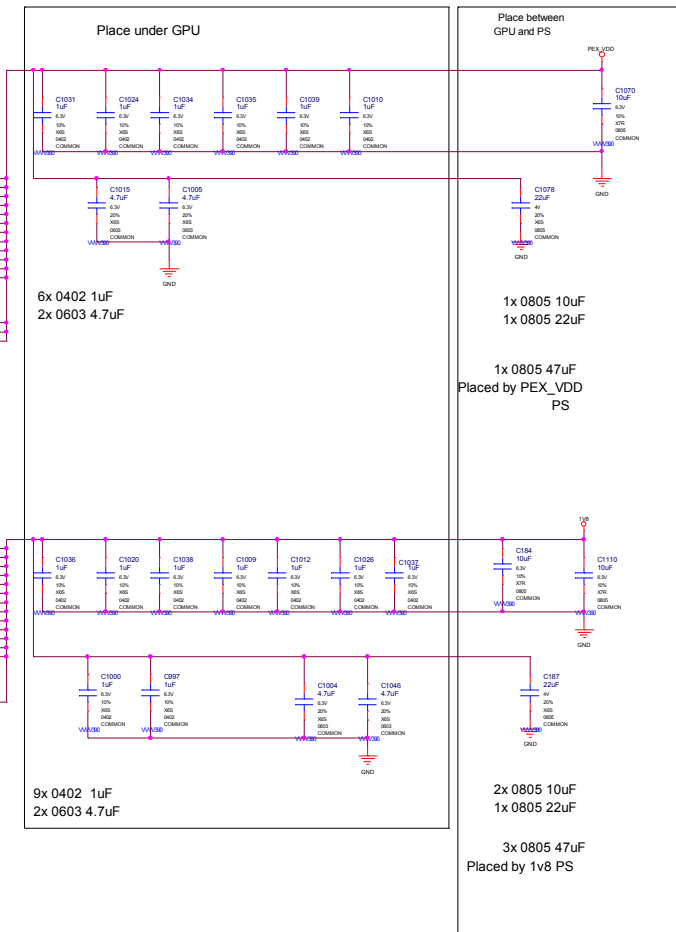
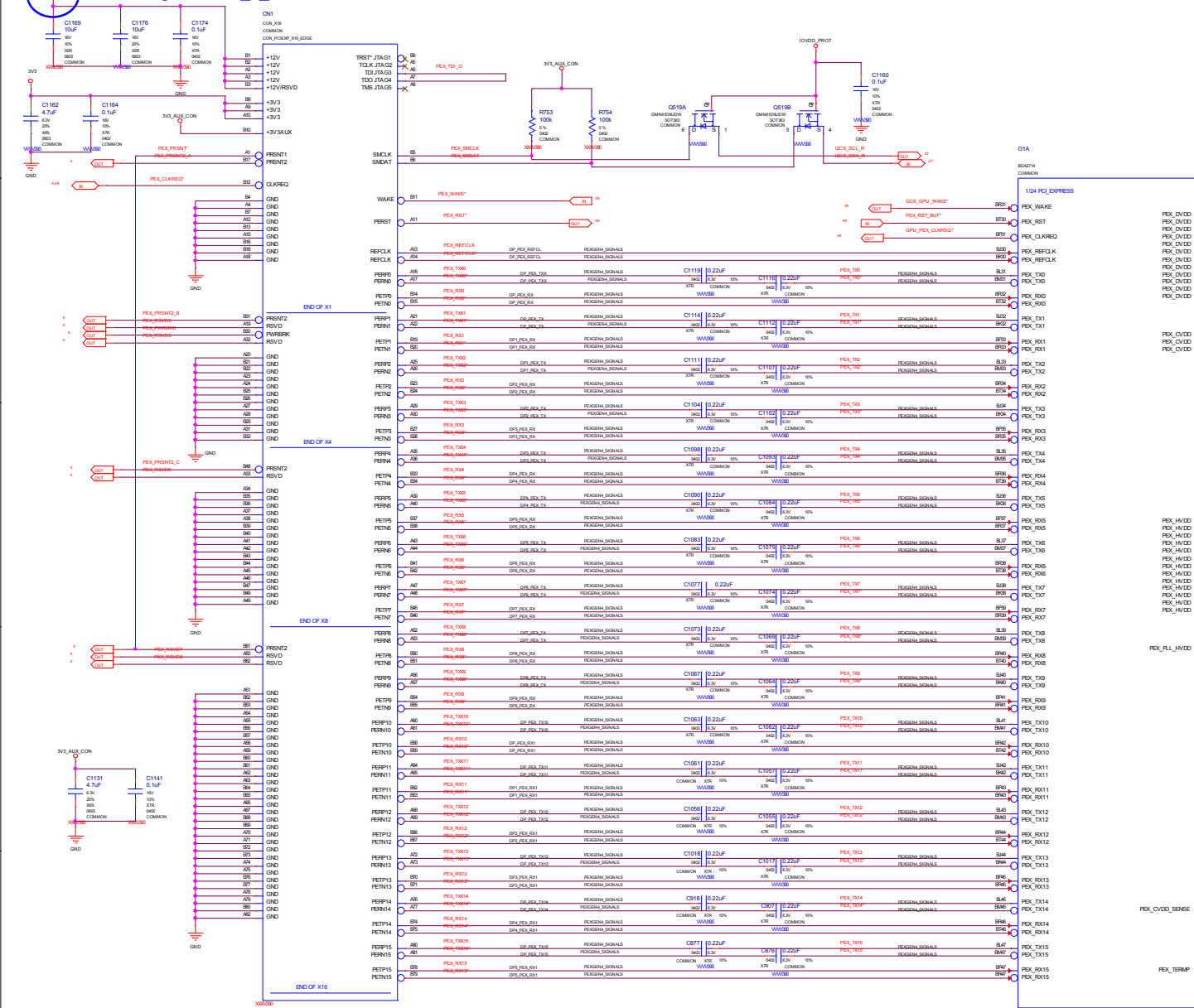
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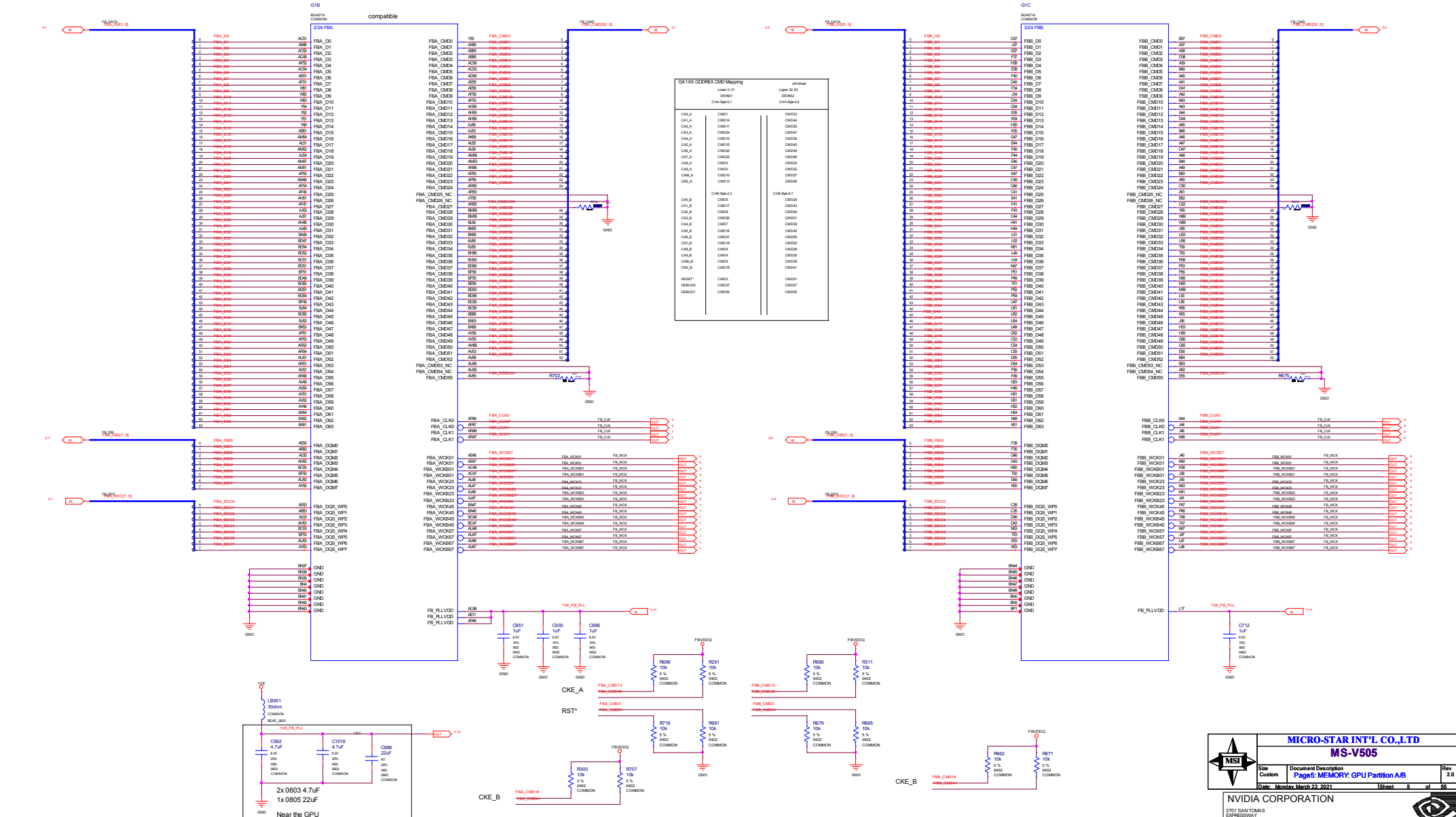
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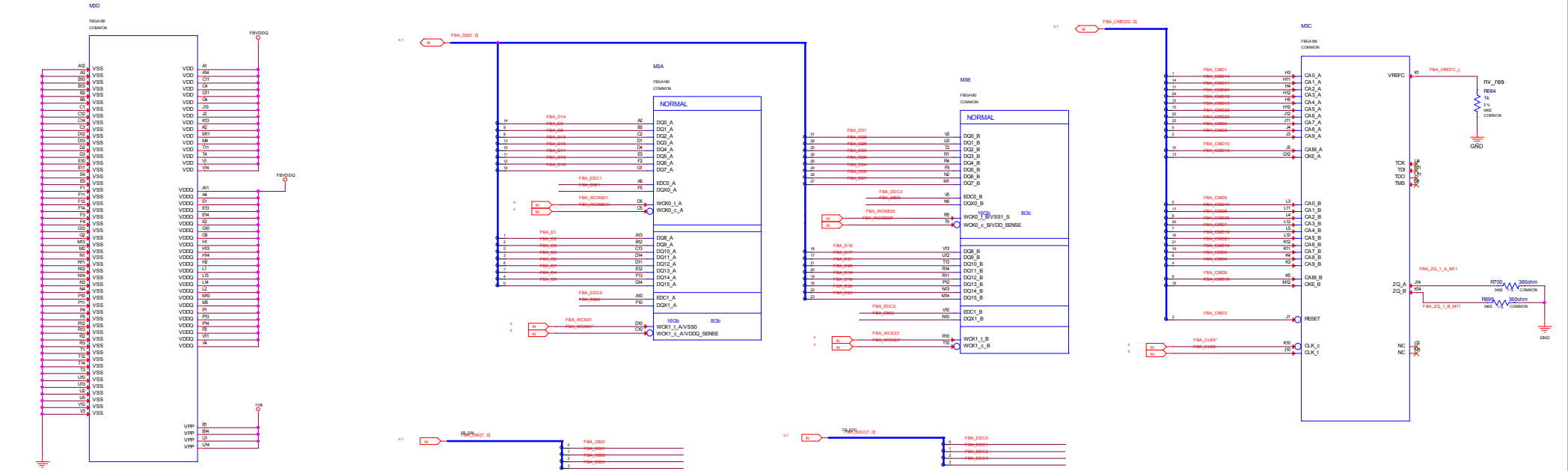
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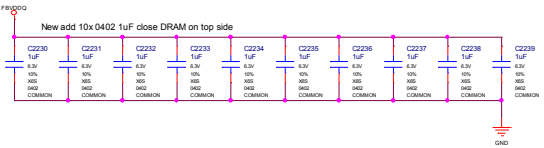
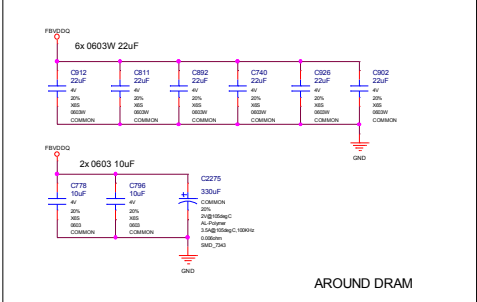
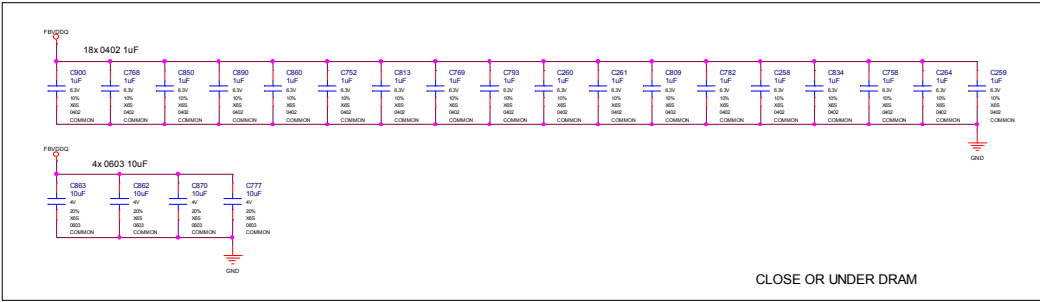
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decap via : at least 2 gnd vias and 2 power vias for each cap



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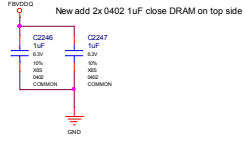
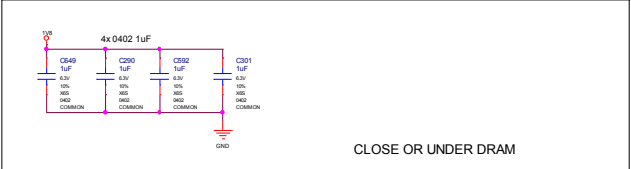
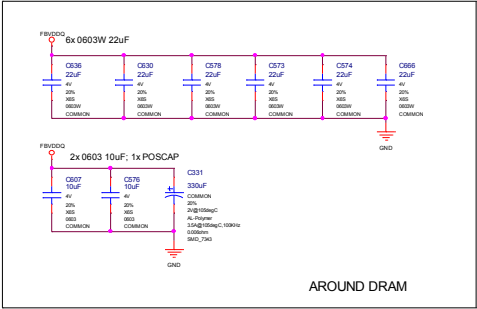
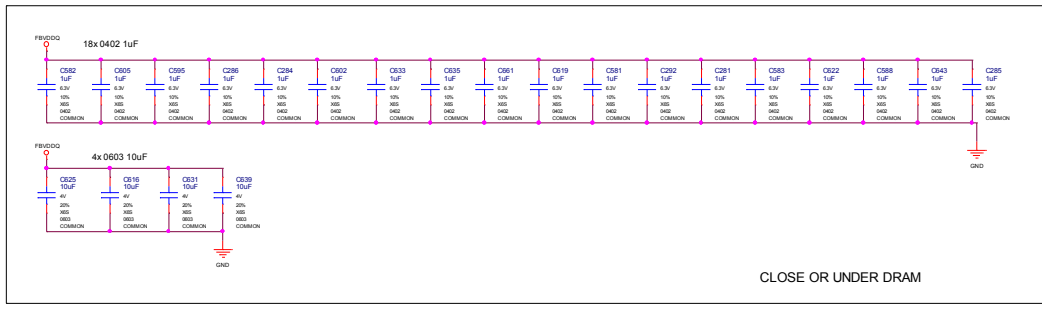
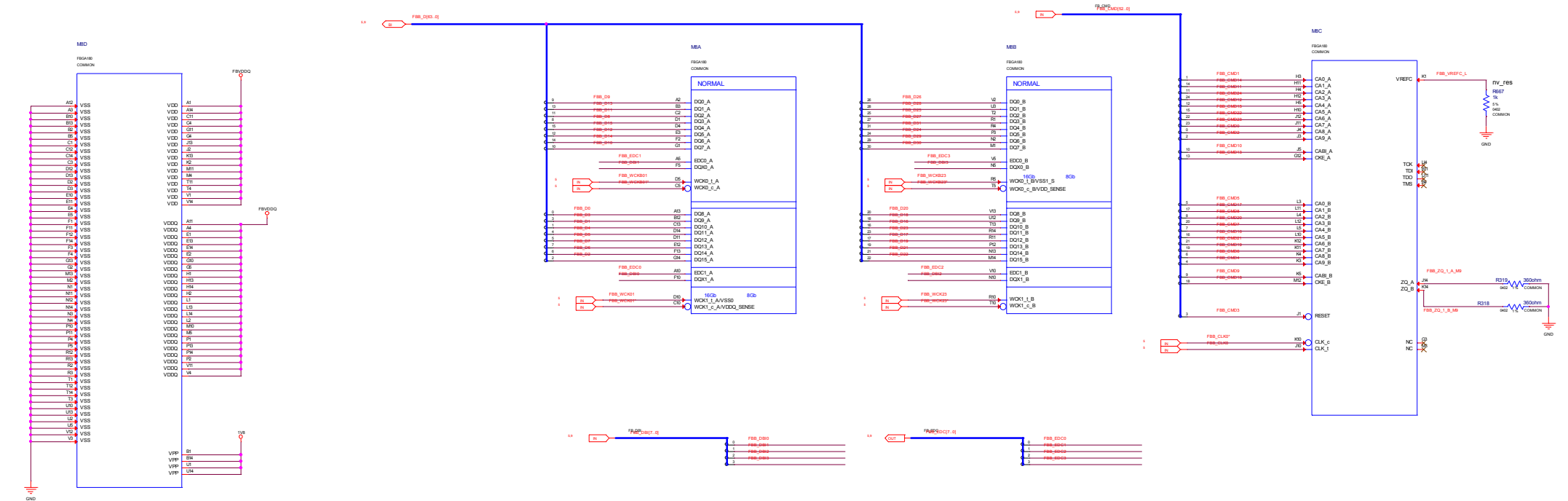
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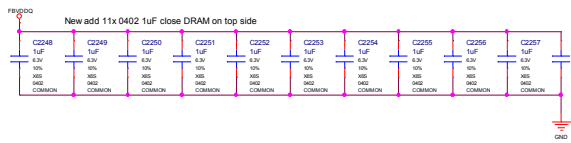
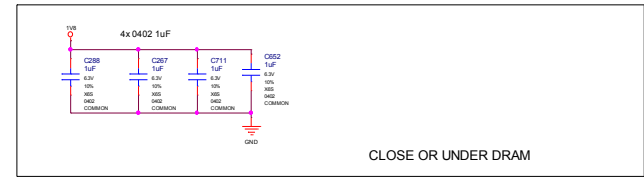
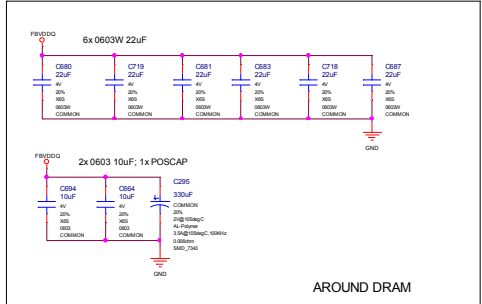
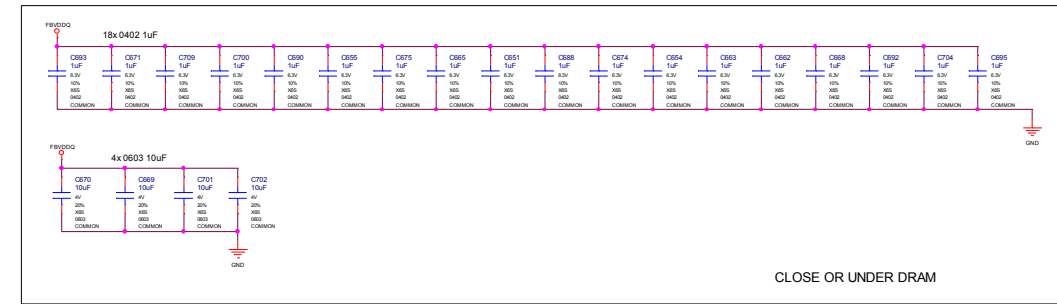
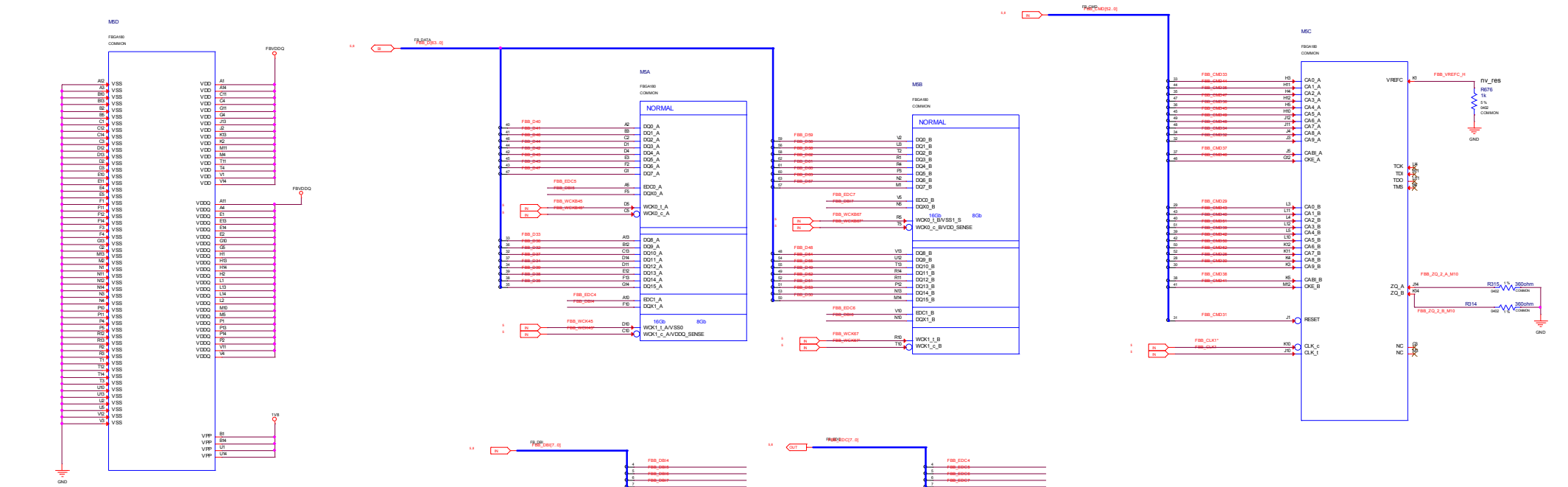
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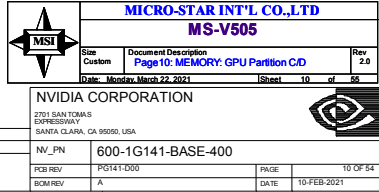
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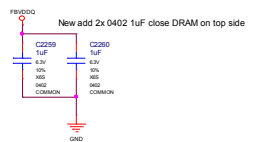
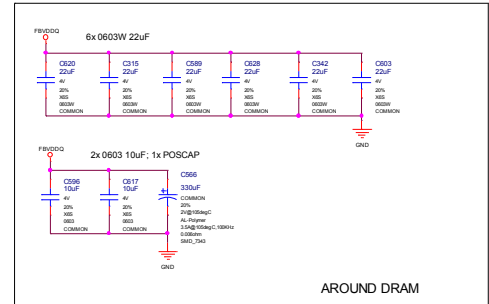
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
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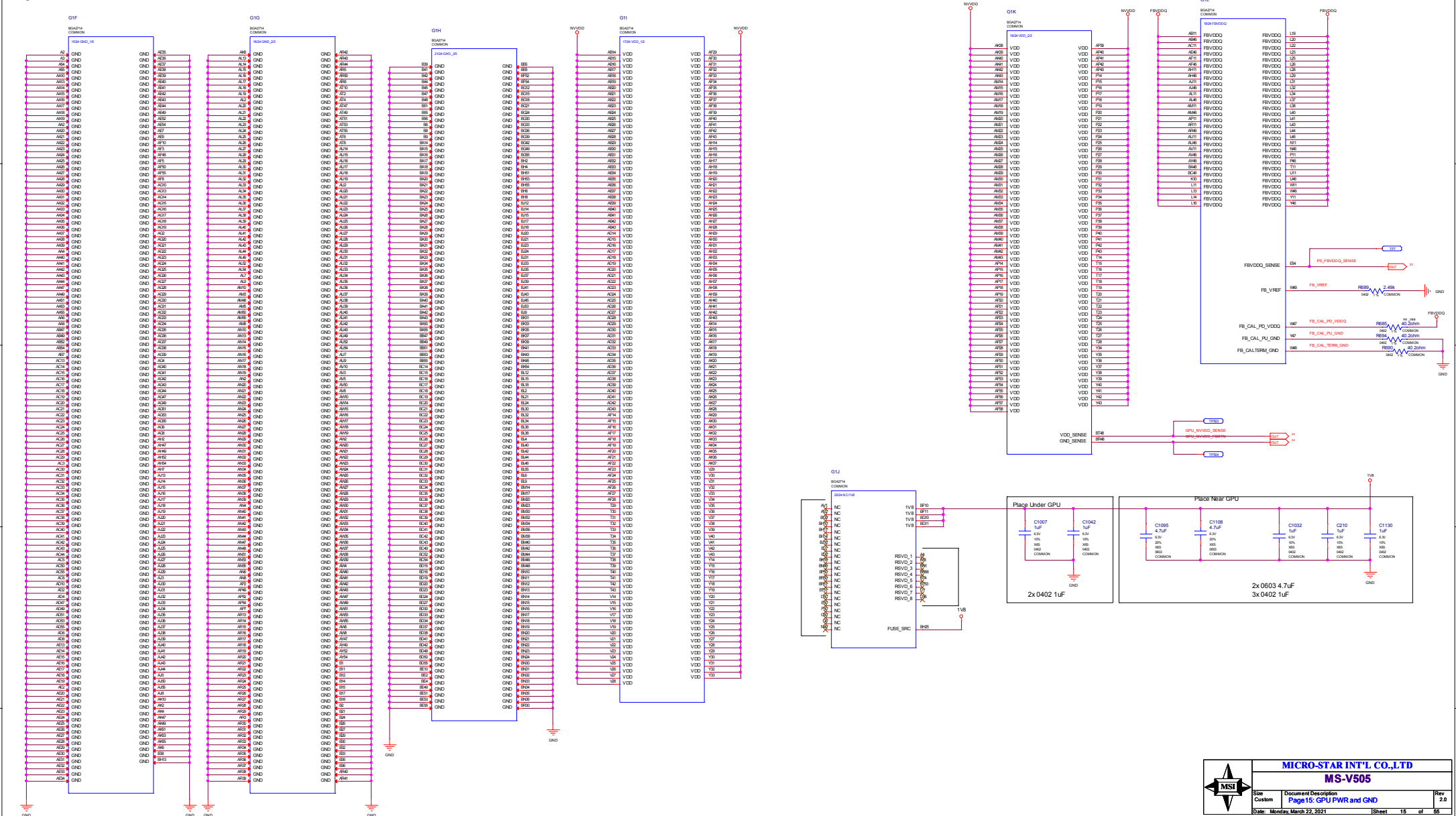
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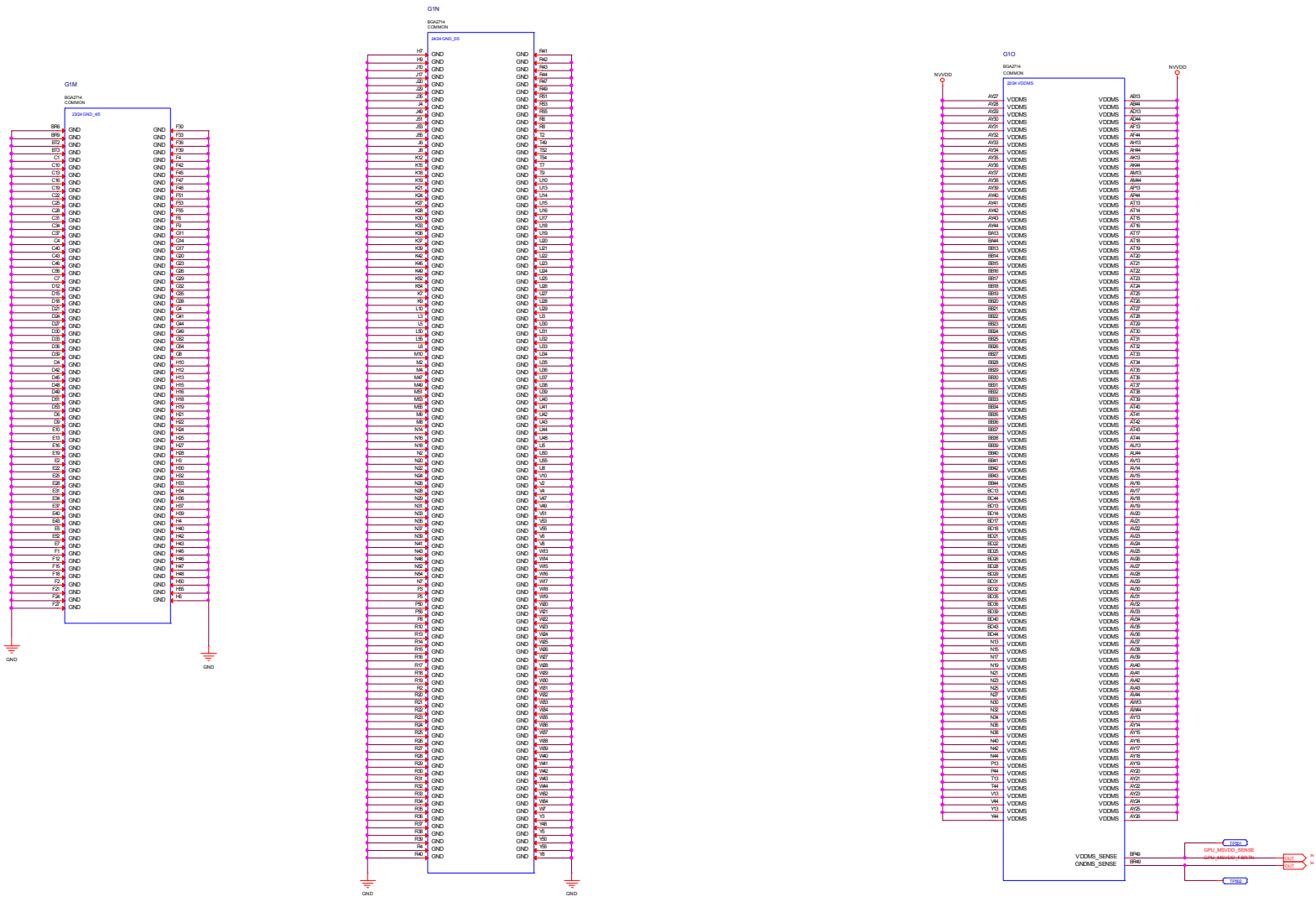


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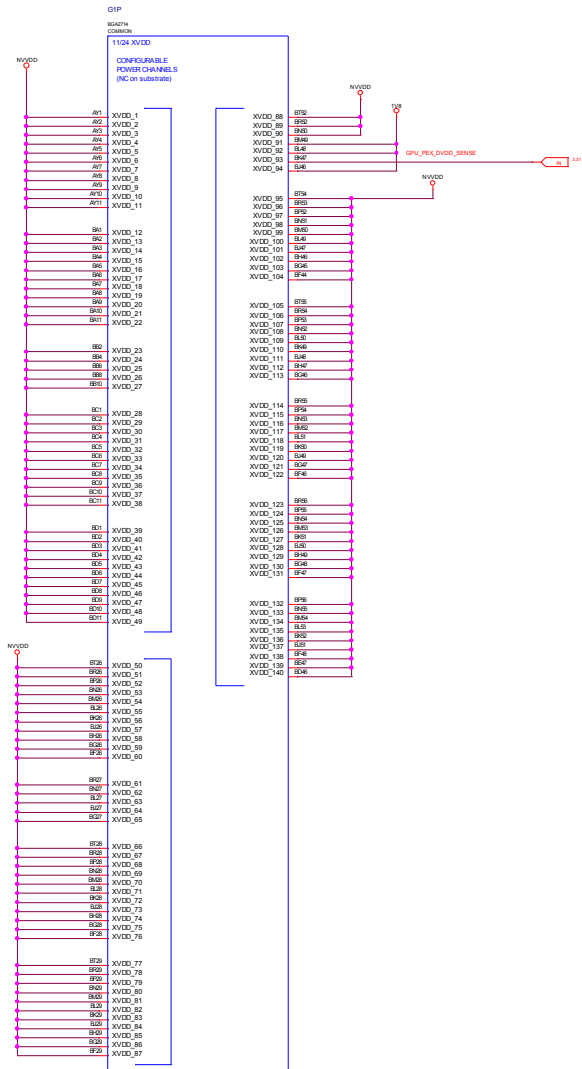
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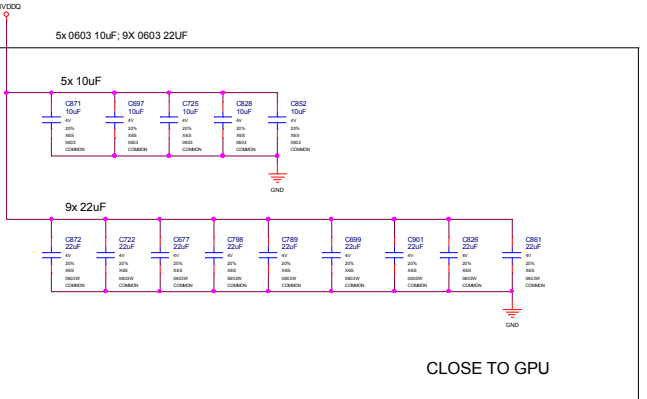
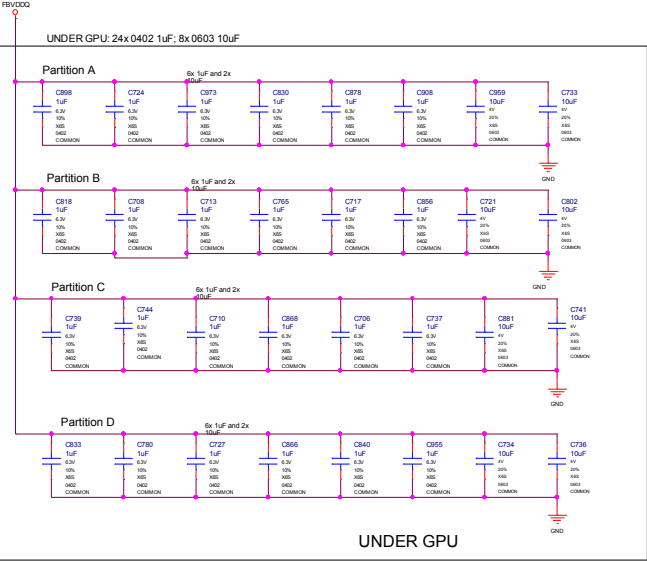
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FBVDDQ





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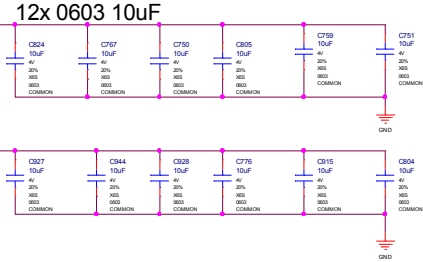
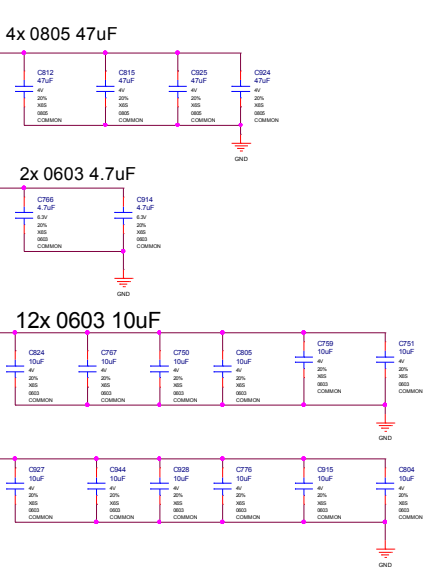
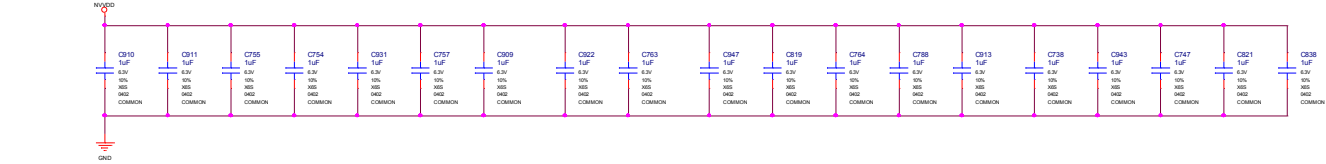
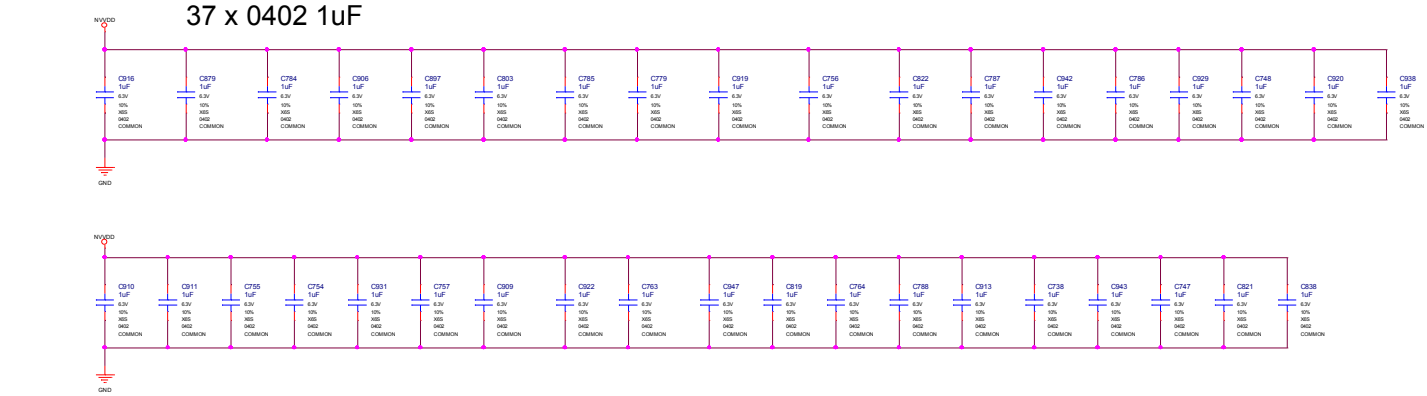
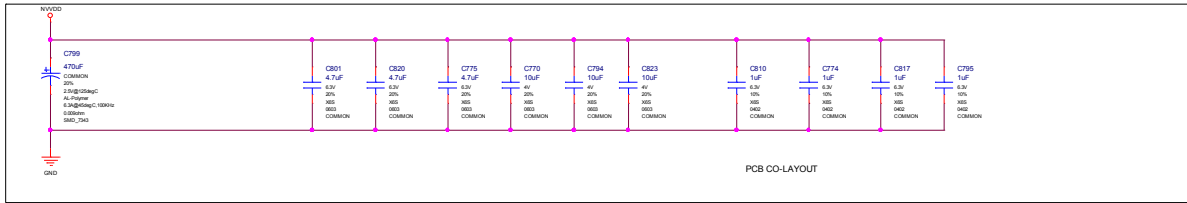
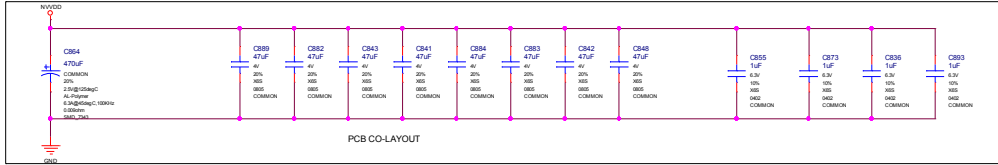
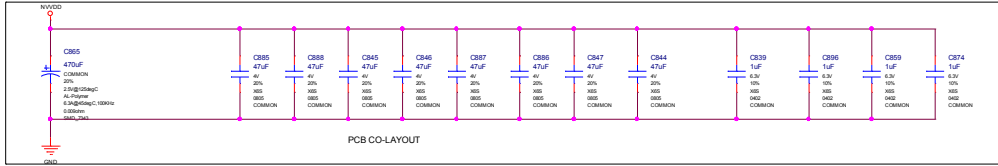
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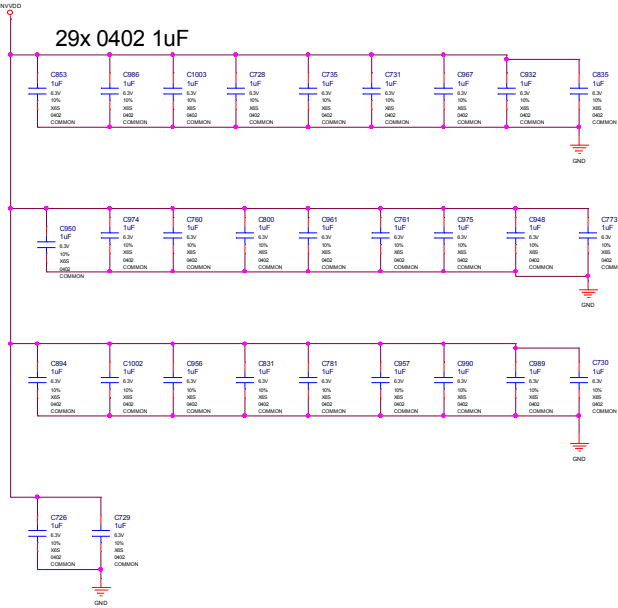
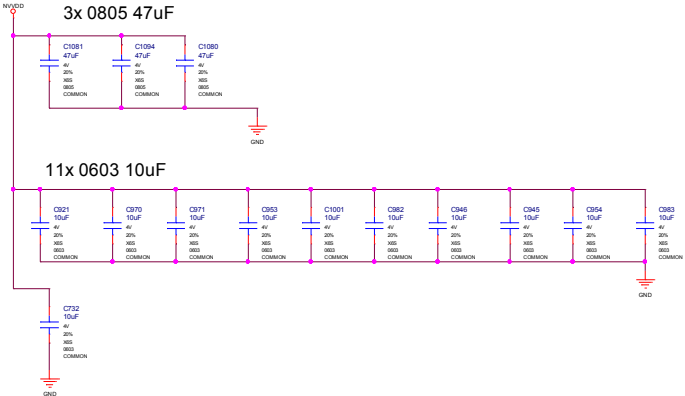
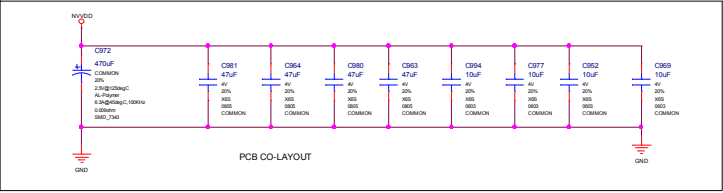
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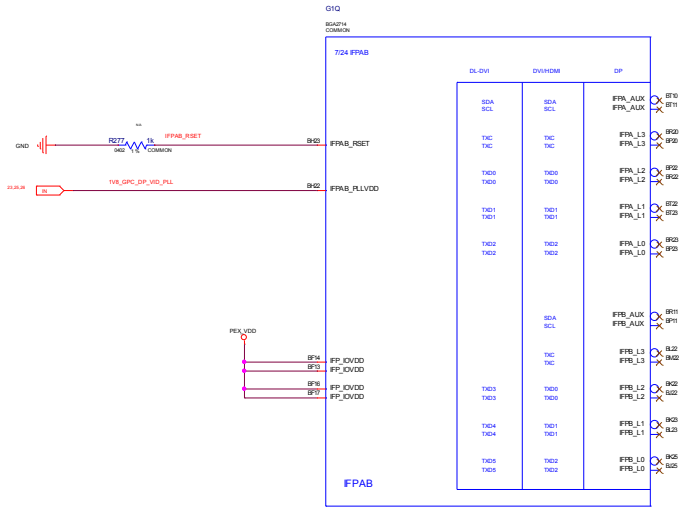
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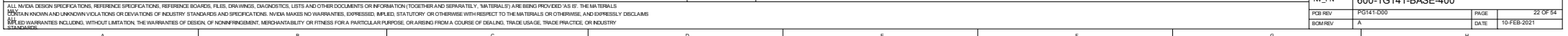
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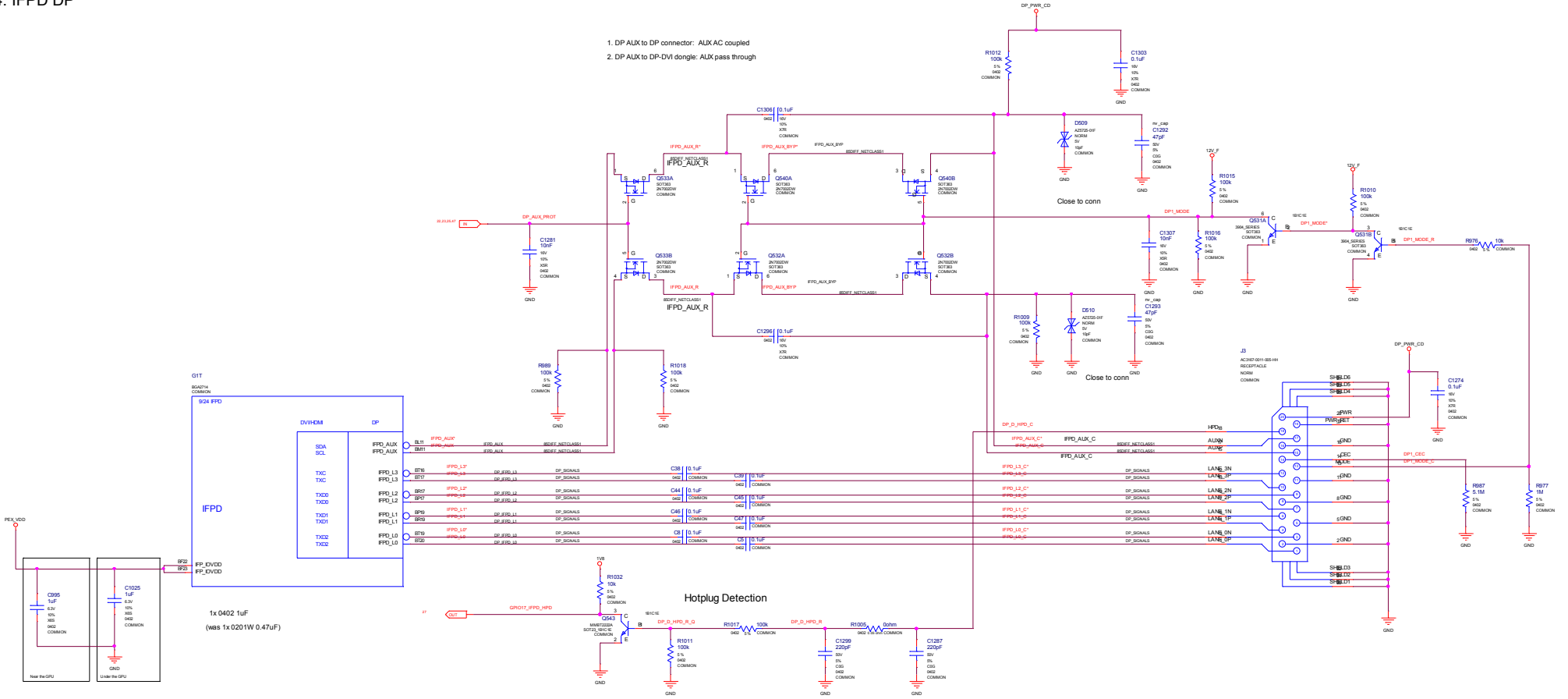
NVIDIA CORPORATION
2701 SAN TOMEAS
EXPRESSWAY
SANTA CLARA, CA 95050, USA

NV_PN	600-1G141-BASE-400		
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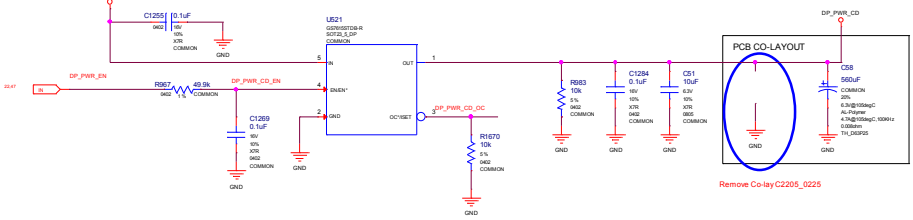
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- 1. DP AUX to DP connector: AUX/KAC coupled
- 2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



Remove Co-Lay C2205_0225




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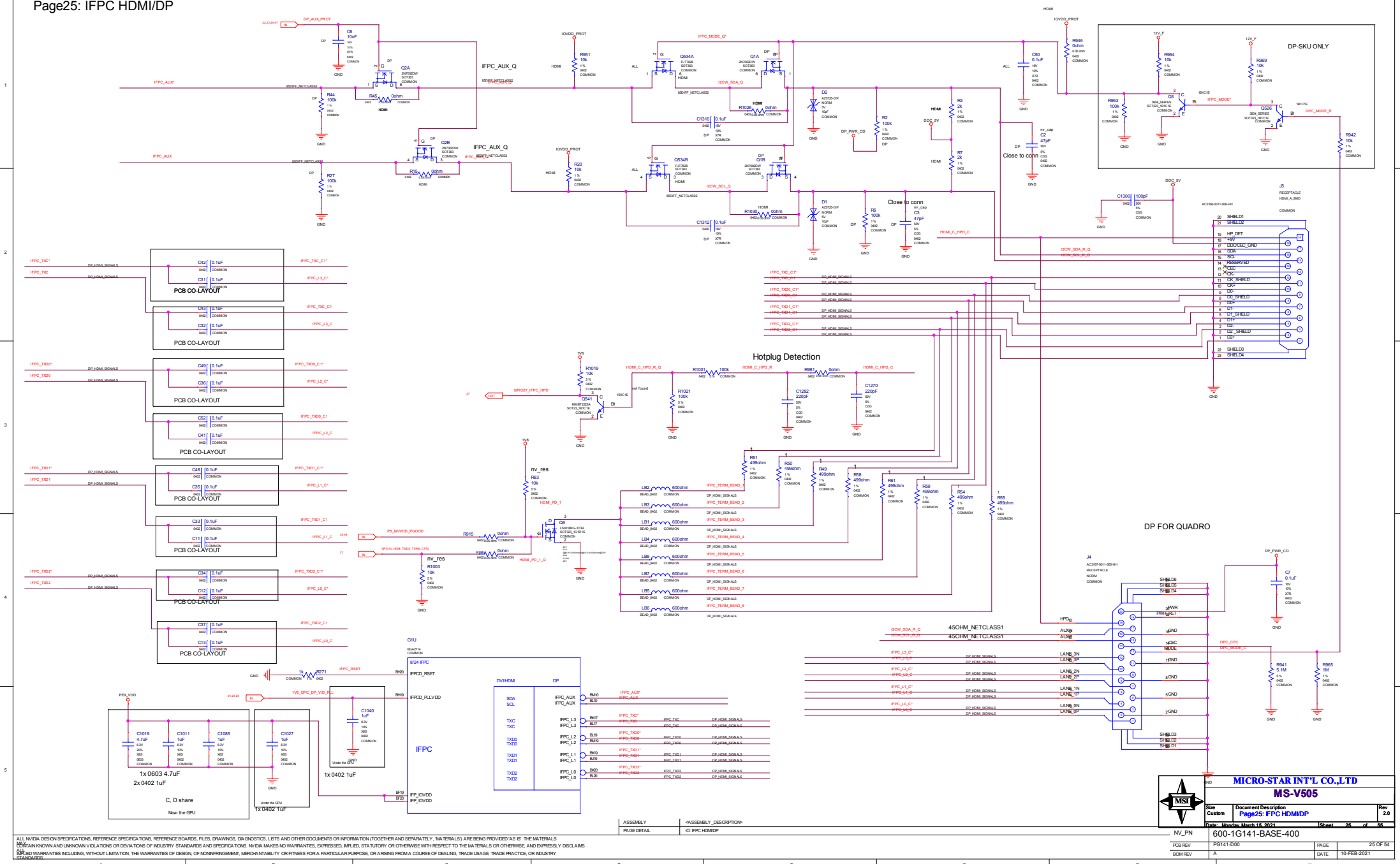
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Date: Monday March 16, 2021

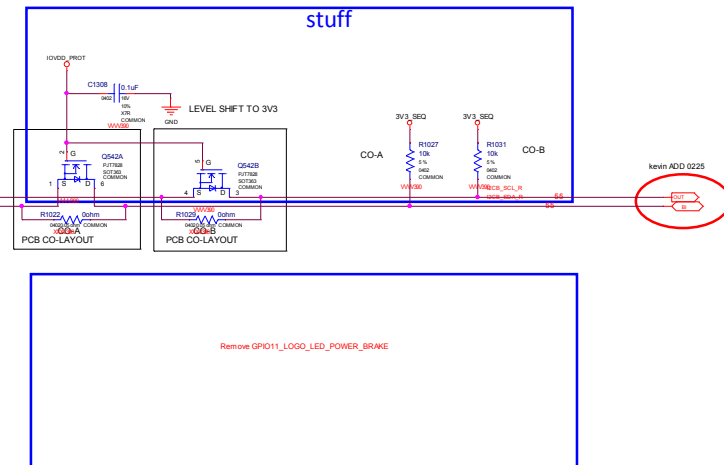
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STEREO

remove STEREO

Remove J6_0225




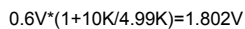
remove LED

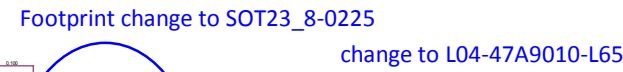
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PAGE DETAIL		MICRO-STAR RGB	



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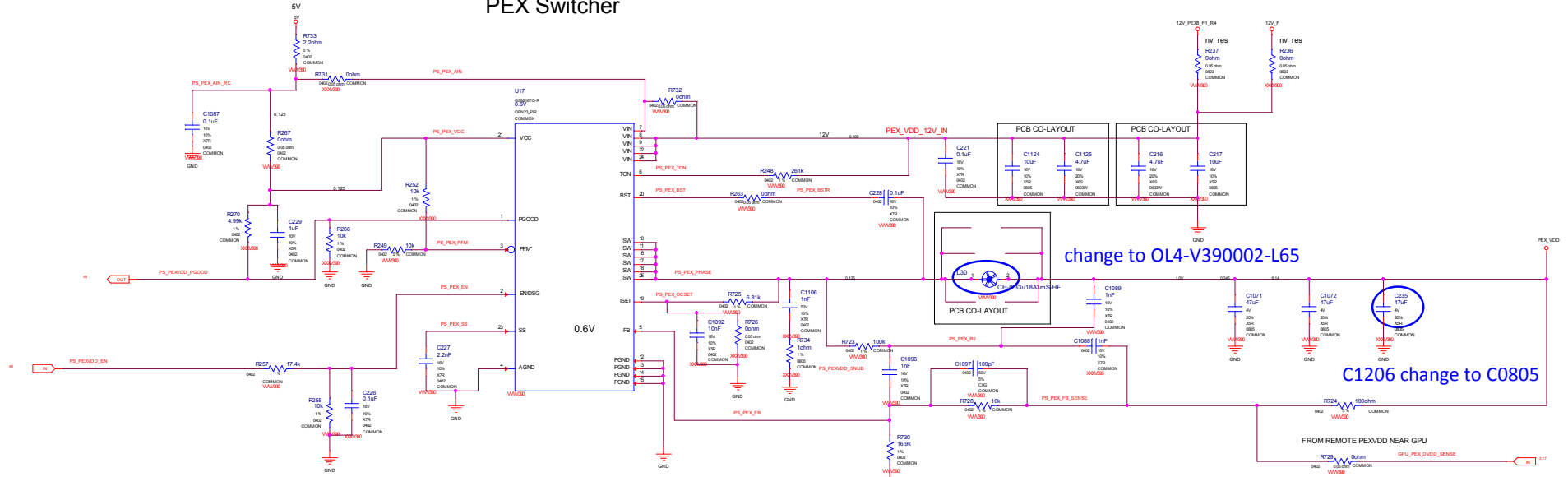




$$0.8V \cdot (1 + 40.2K/7.68K) = 4.9875V$$

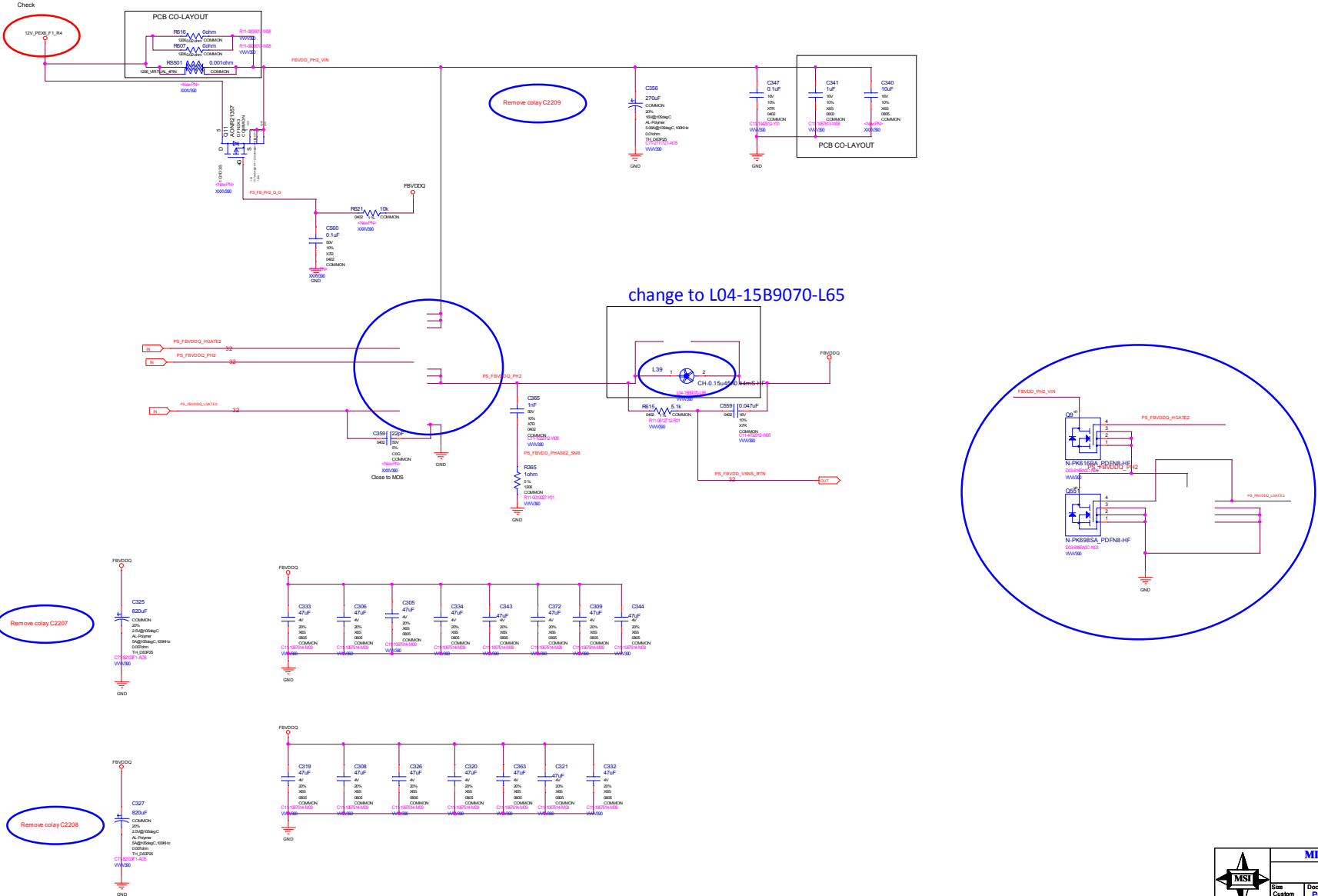
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PEX Switcher



$$0.6V \cdot (1 + 10K/16.9K) = 0.955V$$

FBVDD PH2 INPUT ANTI-BACKDRIVE





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NVVDD PH4(PWM4)

reverse to public board cap

change to OL4-V390003-L65
footprint:public board

delete co-layout MLCC

reverse to public board cap


NVVDD PH6(PWM6)

reverse to public board cap

reverse to public board cap

change to OL4-V390003-L65
footprint:public board

delete co-layout MLCC



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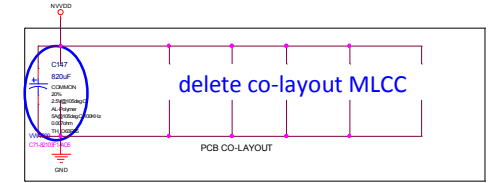
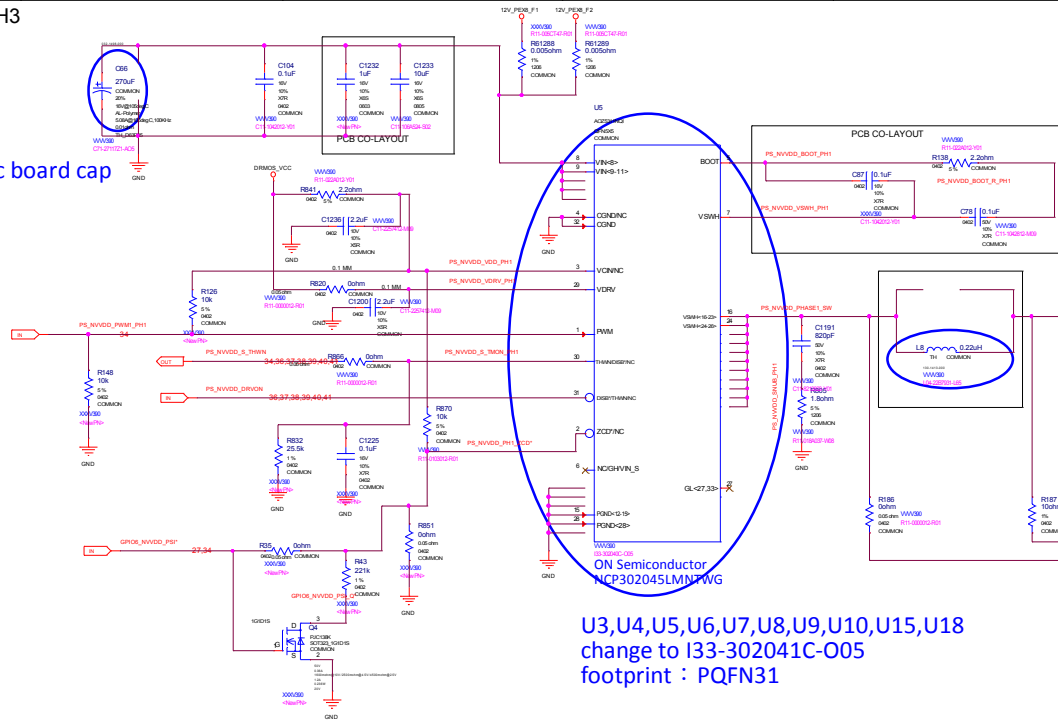
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: NVVDD PH4, PH6

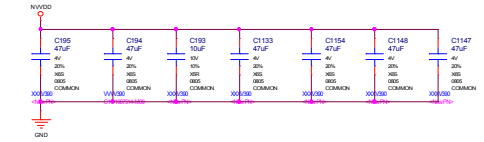
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NVVDD PH1(PWM1)

reverse to public board cap

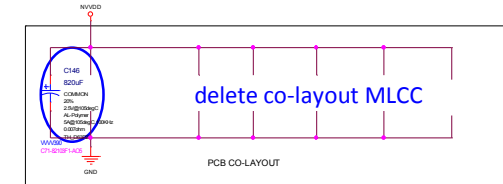
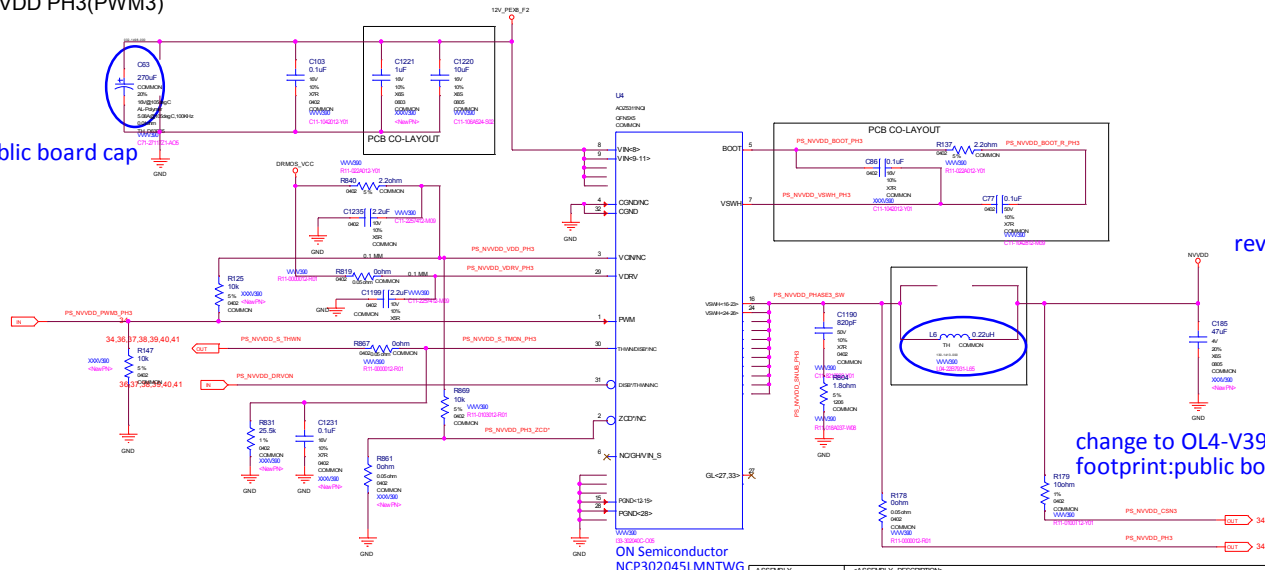


reverse to public board cap

change to OL4-V390003-L65
footprint:public board

NVVDD PH3(PWM3)

reverse to public board cap



reverse to public board cap

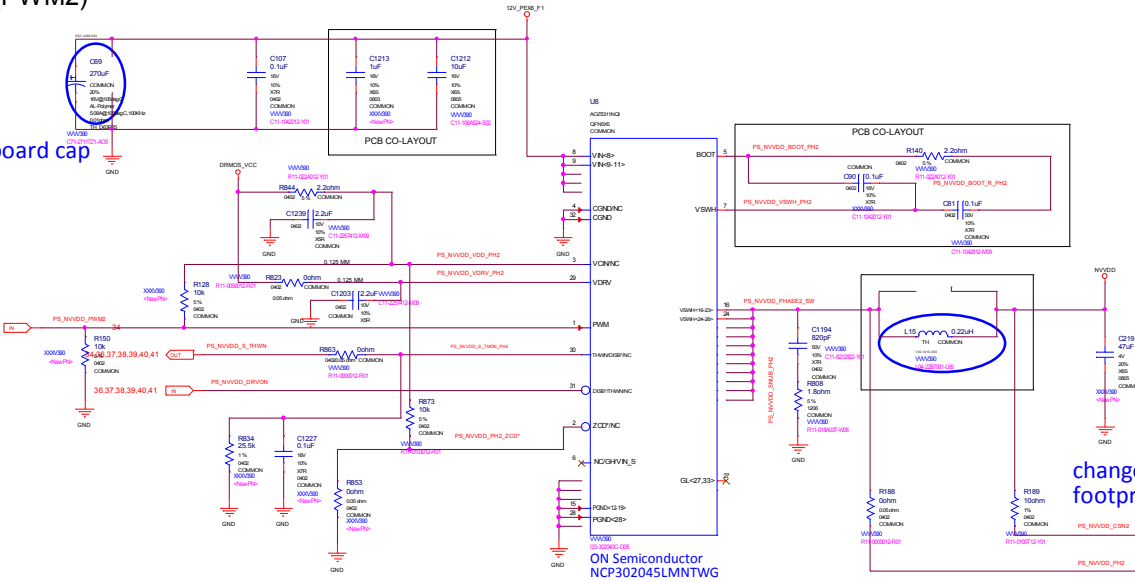
colayout only no self standing mlccs

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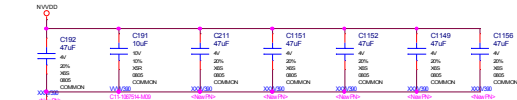
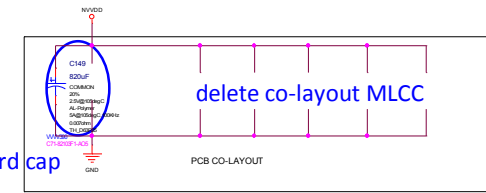
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2701 SAN TOMAS EXPRESSWAY			
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NVVDD PH2(PWM2)

reverse to public board cap

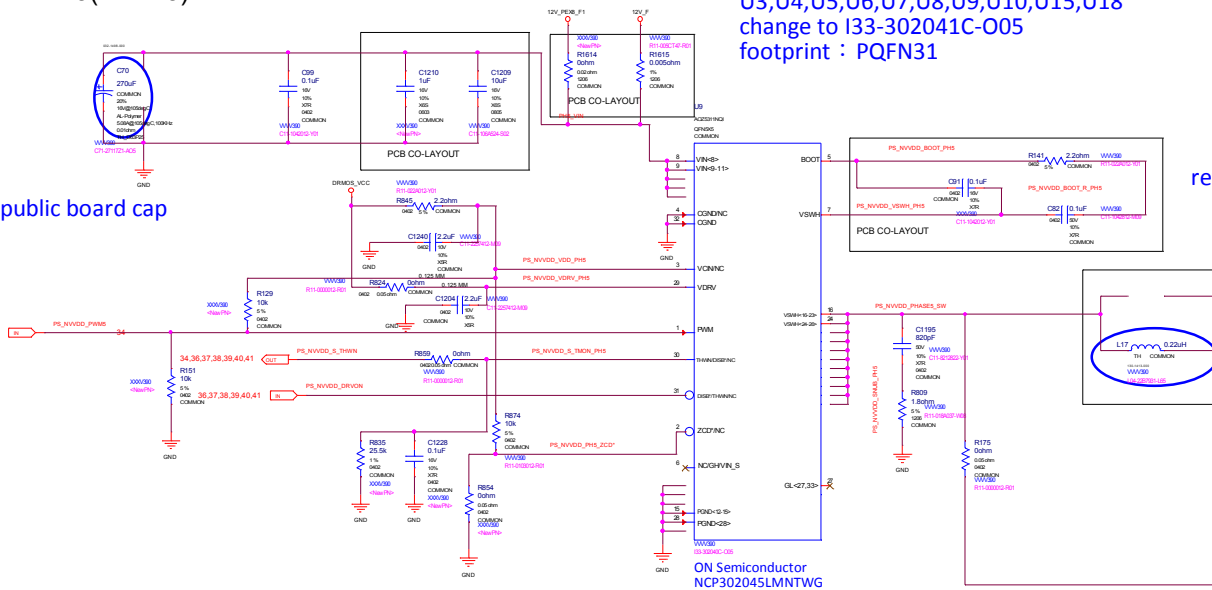


reverse to public board cap



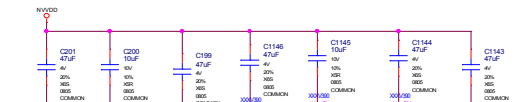
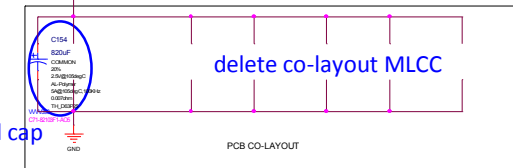
NVVDD PH5(PWM5)

reverse to public board cap



U3,U4,U5,U6,U7,U8,U9,U10,U15,U18
change to I33-302041C-005
footprint : PQFN31

reverse to public board cap

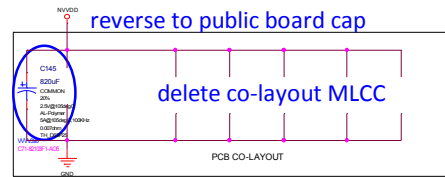
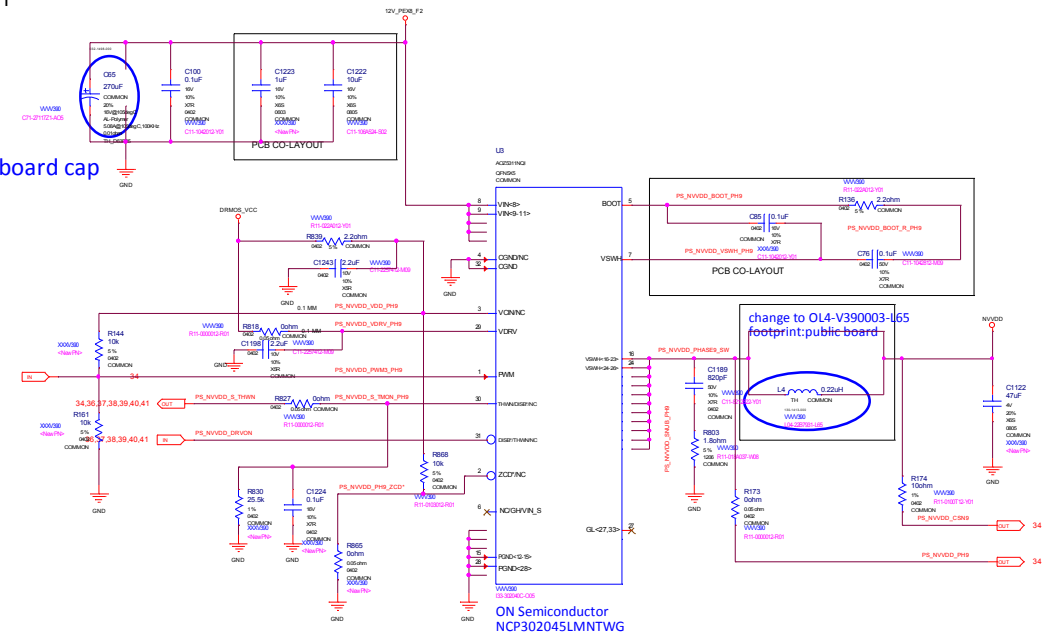


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NV_PN		600-1G142-BASE-100	
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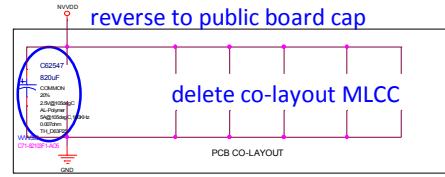
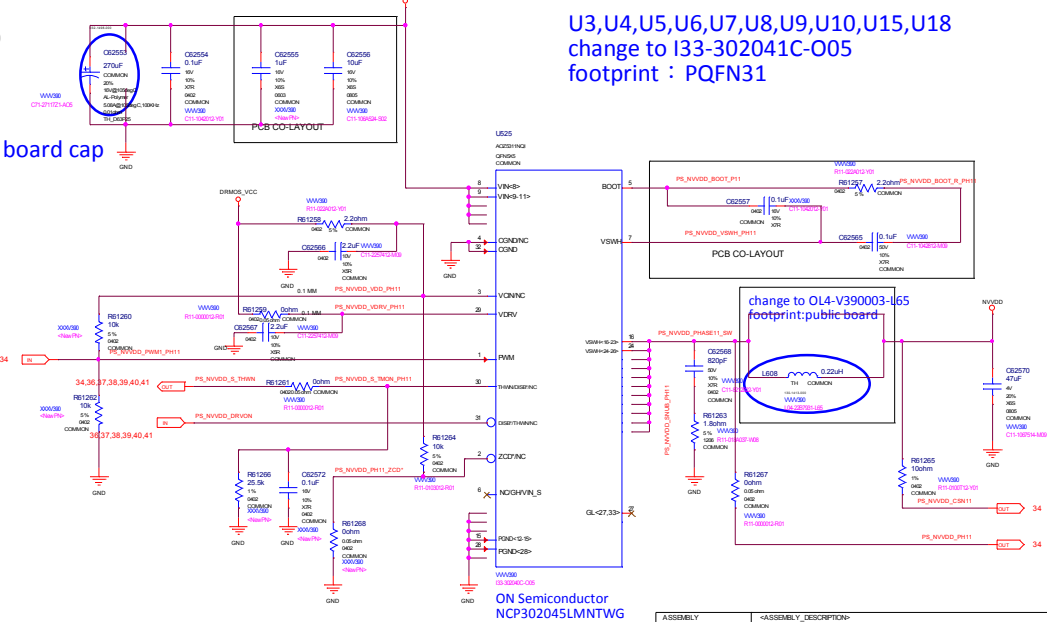
NVVDD PH9(PWM3)

reverse to public board cap



NVVDD PH11(PWM1)

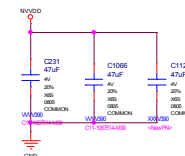
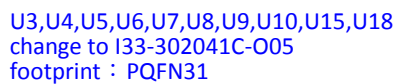
reverse to public board cap



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reverse to public board cap

reverse to public board cap

delete co-layout MLCC

change to OL4-V390003-L65
footprint:public board

NVVDD PH8(PWM8)


reverse to public board cap

U3,U4,U5,U6,U7,U8,U9,U10,U15,U18
change to I33-302041C-005
footprint : PQFN31

reverse to public board cap

delete co-layout MLCC

change to OL4-V390003-L65
footprint:public board

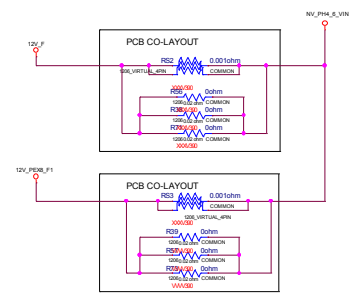
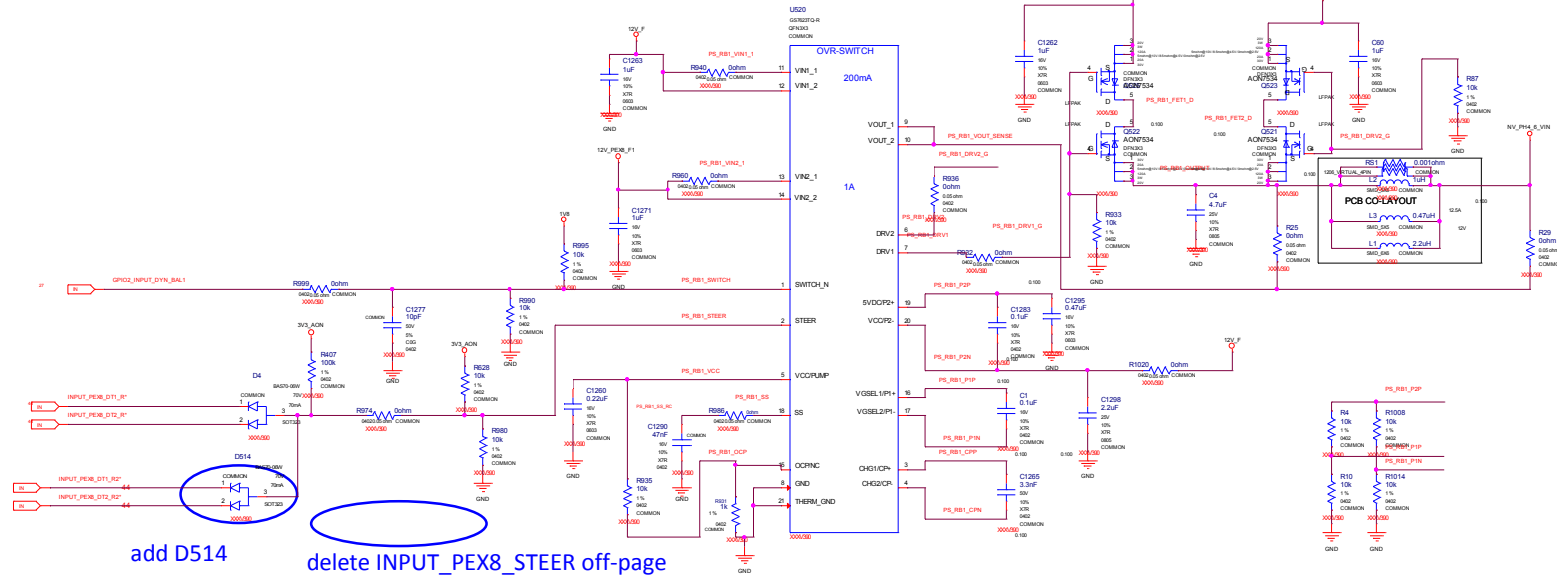
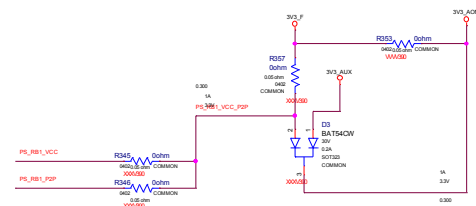


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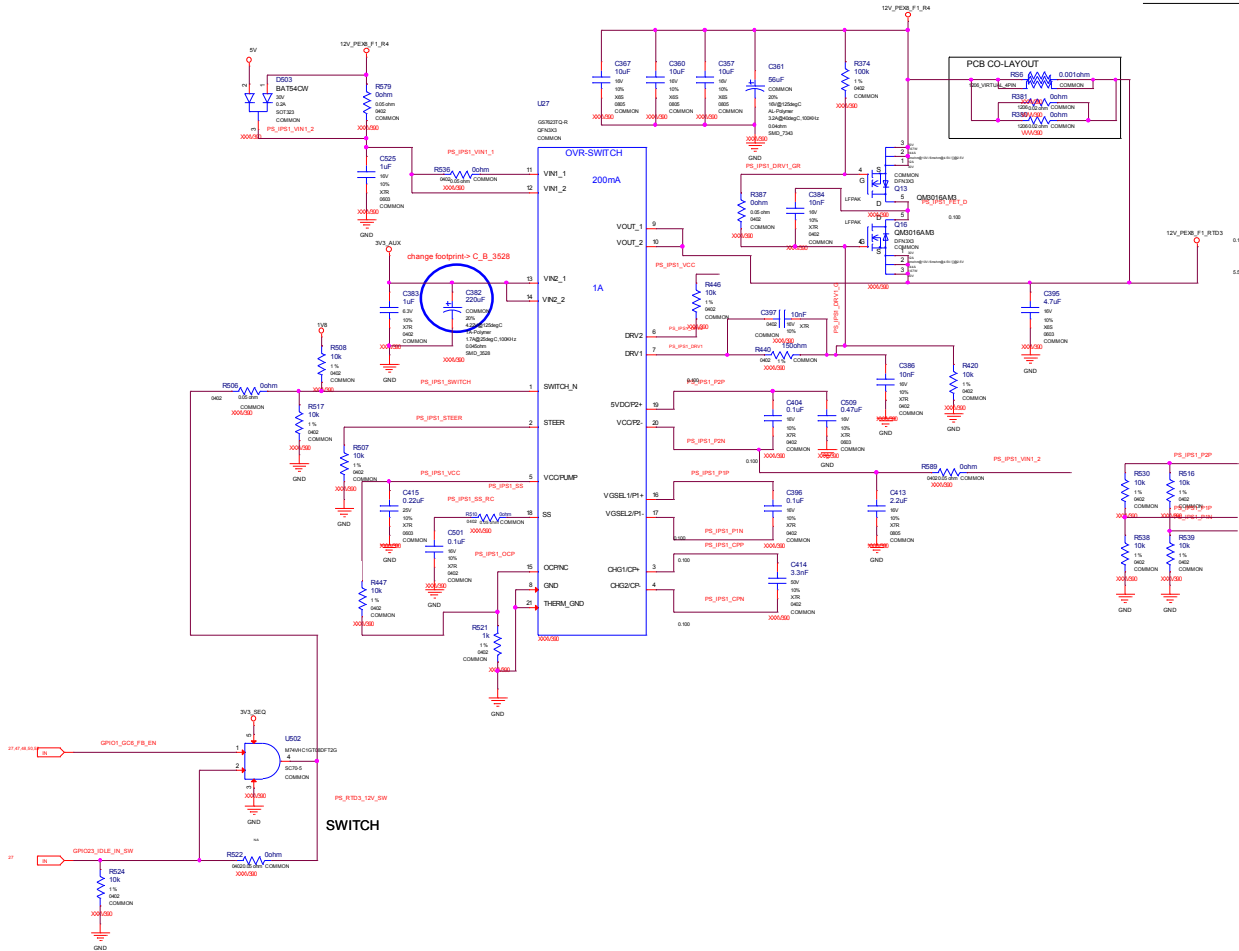
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: NVVDD PH10, PH8

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AND GATE LOGIC					
GPI01	GPI023	SWITCH	VOUT	SWITCH	VOUT
0	0	0	12V	0	VOUT = VIN1
0	1	0	12V	1	VOUT = VIN2
1	0	0	12V		
1	1	1	3V3A		





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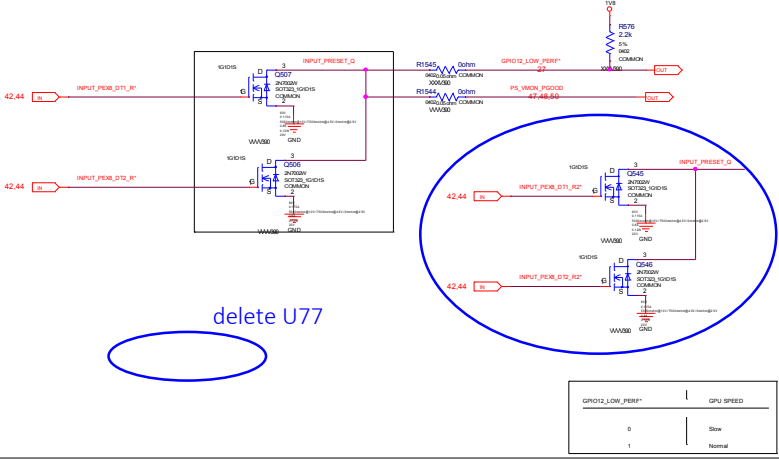
ASSEMBLY	ASSEMBLY DESCRIPTION
PRG DETAIL	PS: RTD3, 12V & 3V3_A Switcher

delete 12 pin 12V EXT-POWER Current steering

ADD power tree 0317

12V_F(RSENSE 1) EXT1-12V_PEX8_F1(Rsense 2)->NV_PH4_6_VIN
->NV5,NV8 NV2 NV4,NV6
EXT1-12V_PEX8_F2(RSENSE 3) NV1,NV3,NV7,NV9,NV10,NV11
->12V_PEX8_F1_R4(Rsense4) -->12V_PEX8_F1_RTD3
PEX_VDD,FB2 IV8,5V,FB1

PEX Input - Under Power Boot Control



delete U77

PEX8 INPUT 2/B - 2x4 PCIE CON 150W

Fuse

PCB CO-LAYOUT

F7 FUSE 250V 5010269-HF

delete R2007

Fuse

PCB CO-LAYOUT

F9 FUSE 250V 5010269-HF

delete R2010

PEX8 INPUT 1/A - 2x4 PCIE CON 150W

Fuse

PCB CO-LAYOUT

F7 FUSE 250V 5010269-HF

delete R2007

Fuse

PCB CO-LAYOUT

F9 FUSE 250V 5010269-HF

delete R2010

PEX 8 Input Present 1/A

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

PEX 8 Input Present 1/A

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

INPUT_PEX8_DT1_R1

INPUT_PEX8_DT1_R2

INPUT_PEX8_DT2_R1

INPUT_PEX8_DT2_R2

one 12pin EXT power conn. change to reverse 8pin conn.

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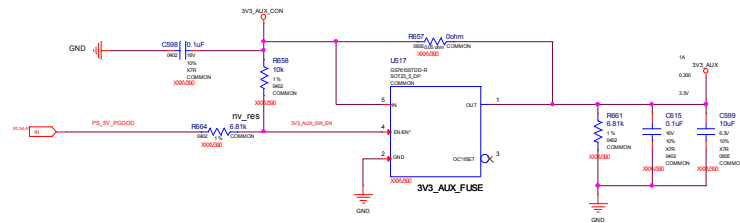
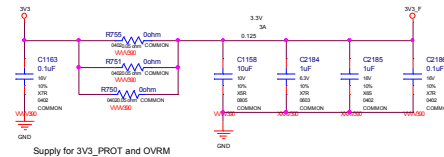
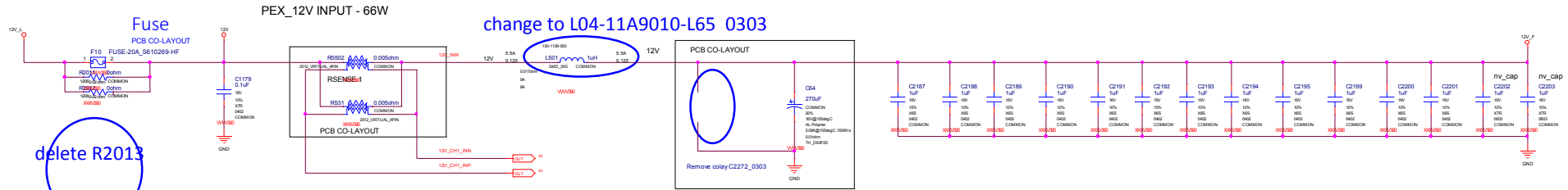
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
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DATE 27-JUN-2020



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POWER CONNECTOR HOT-UNPLUG DETECT


delete POWER CONNECTOR HOT-UNPLUG DETECT

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

delete 12V CURRENT STEERING

ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB, HOT UNPLUG



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Size

Custom

Document Description

STEERING, UPB, HOT UNPLUG

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P0141 D00

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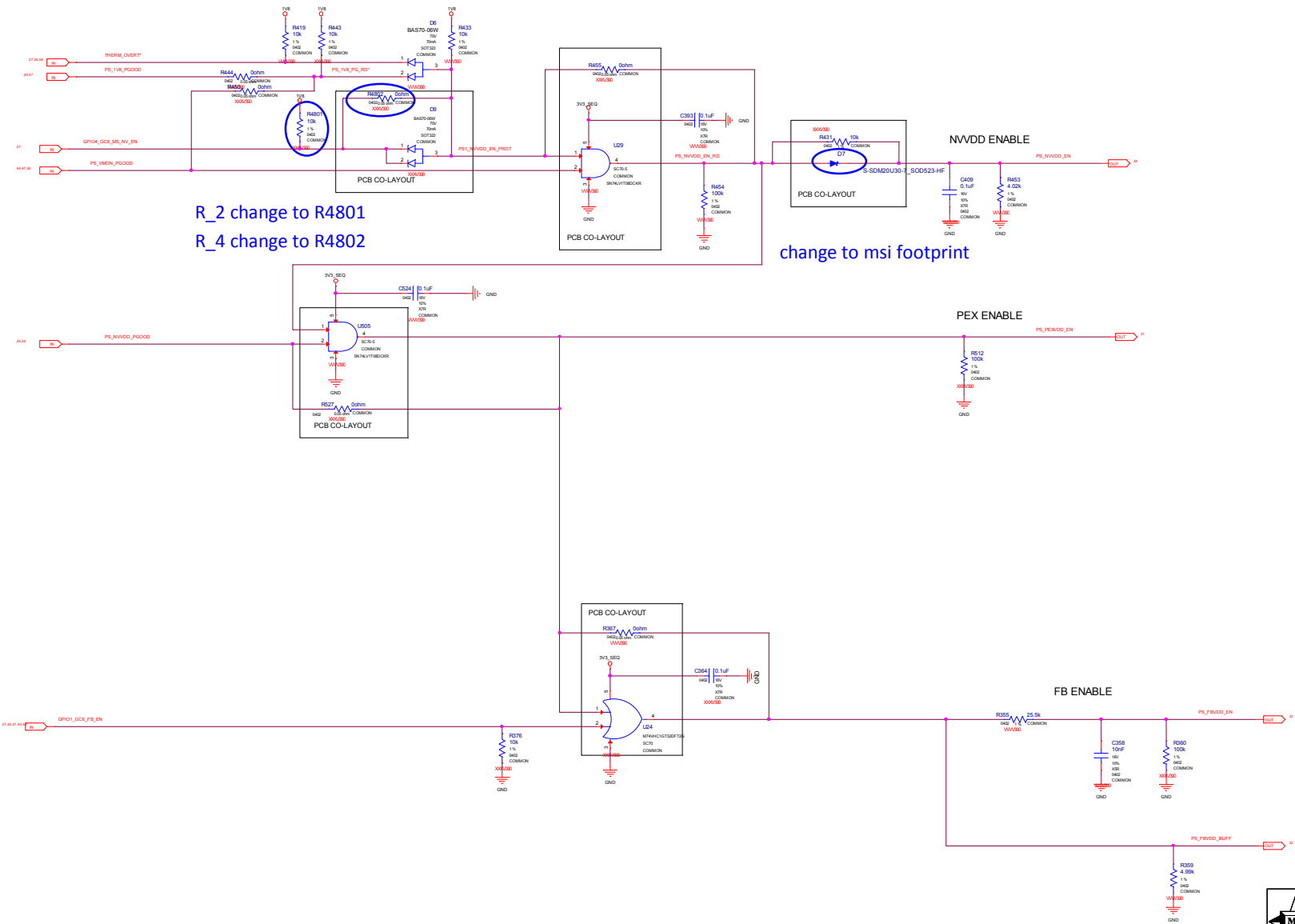
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A


DATE

10-FEB-2021



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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	SEQ NVVDD, PEX, FBVDDQ ENABLE



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Size: Custom

Document Description: SEQ NVVDD, PEX, FBVDDQ ENABLE

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2701 SAN TOMAS EXPRESSWAY

SANTA CLARA, CA 95050, USA



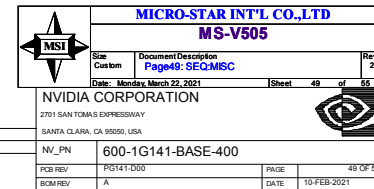
NV_PN: 600-1G141-BASE-400

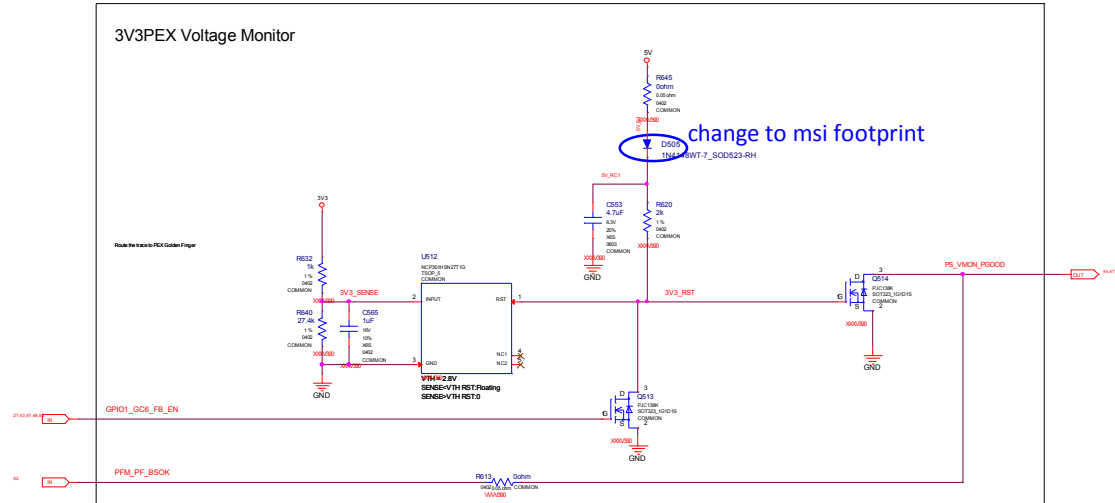
PCB REV: P0141 D00

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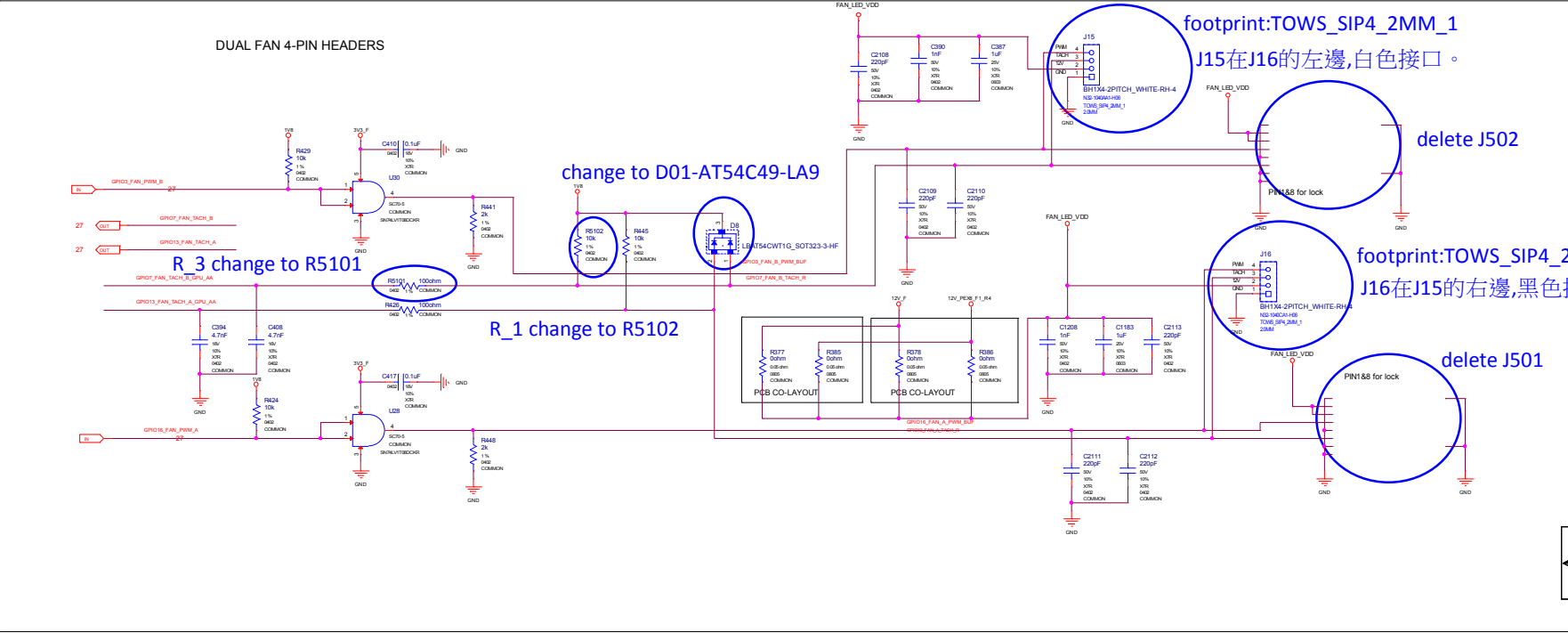
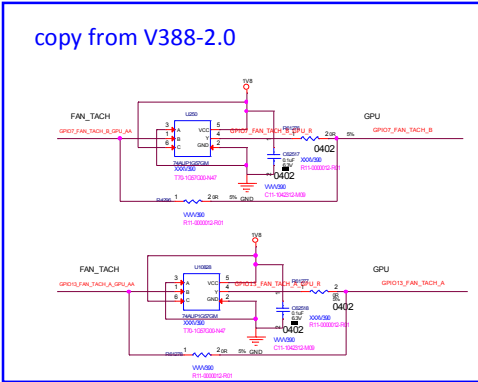




Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(!) once both 3V3 and 12V reach Vth
GCS_FB_EN	INPUT	Indicator for RTD3/GCS resistance Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221 (VPU) or Pre-filter (SKIP)
PS_PF_BSOK	INPUT	From INA3221 (PV) or Pre-filter (BS_OK)

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		Size Document Description Rev		
		Page 50: SEQUENCE/Voltage Monitor		
		Date: Monday, March 22, 2021	Sheet 50	of 55
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2-PIN LED HEADER
remove 2-PIN LED HEADER



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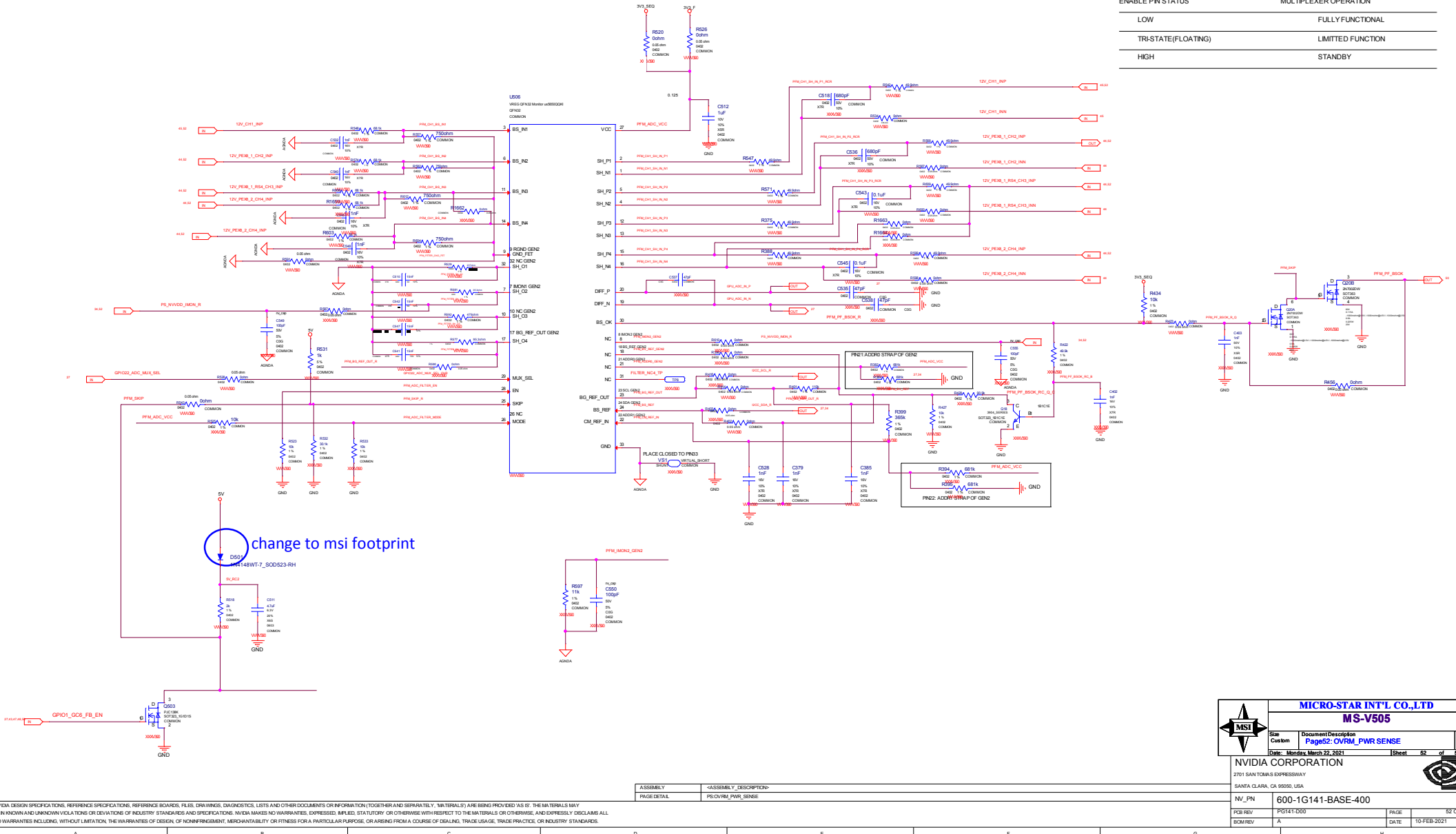
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Site: Custom
Document Description: 0051_FAN & LED
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PCB REV: P0142-800
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	FAN & LED

MODE PIN STATUS		MULTIPLEXER OPERATION	
LOW		DEVICE A	
TRI-STATE(FLOATING)		STAND-ALONE	
HIGH		DEVICE B	

ENABLE PIN STATUS		MULTIPLEXER OPERATION	
LOW		FULLY FUNCTIONAL	
TRI-STATE(FLOATING)		LIMITED FUNCTION	
HIGH		STANDBY	





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Size: Custom

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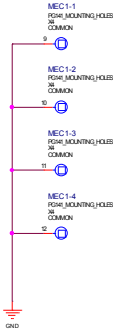
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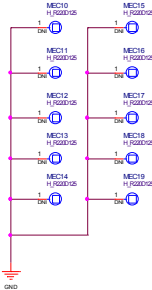
Bracket & Bracket hole: 2pcs
footprint:H_R220D125



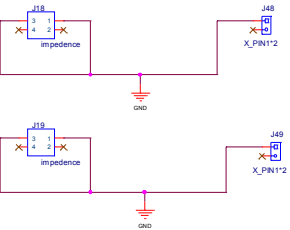
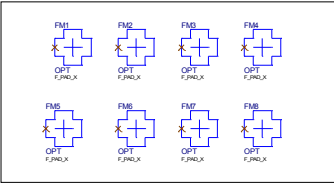
Fan module hole: 4 pcs
footprint : same as public board



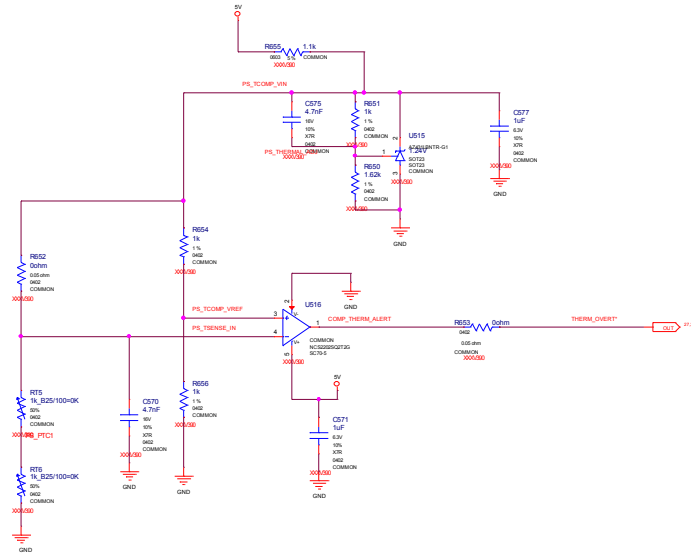
Fan module hole: 10 pcs
footprint:H_R220D125




删除CLP1~CLP3



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		MS-V505	
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PTC

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	Size	Document Description	Rev
	Custom	PTC	1.0
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Nv_PN PCH REV MBM REV A	600-1G141-BASE-400 P0141-D00		PAGE DATE
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debug, not stuff.

LED_A

J5009在J5010的左邊,紅色接口。

LED_B

J5010在J5009的右邊,黑色接口。

LED_C

Remove LED *6 (LED_D) kevin

debug, not stuff.

銷庫存MCU料號

J1022不上件。 kevin ADD J1023 0225

(option)

reserve, not stuff.

change to L04-47A9010-L65

ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: NV LED Controller

SOT223
315-0770-000
315-0767-000

Vout=1.25*(1+1020/340)+60uA*1020=5.06V

MSI		MICRO-STAR INT'L CO.,LTD	
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